Description Title of Invention:

1. COMBINATORIAL LOGIC GATES CIRCUITS MADE WITH ANY CONDUCTOR MATERIAL AT ANY POSSIBLE SIZE ENABLING LIGHT SPEED.

Technical Field

2. Fields of the invention include digital circuits, foundations of computer architecture, simplification of a universal logic gate, first order logic, materialization of software/algorithms and networking.

Background Art

3. Relays, vacuum tubes and semi-conductor transistors where used as inner circuit switches to make universal logic gates.The logic gate NOR is known to be universal as much as the logic gate NAND. One of those universal gates when used many time in a structure can make a processor or materialize an algorithm.

There are less standard ways to make a universal logic gate like carbon transistors, molecular, thermal, DNA, chemical, bio-molecular or ring resonator based universal logic gates.But none is with the simplicity of composing any conductor to make any combinatorial logic gates circuit.

Summary of Invention

4. Using special switches at the surface of the circuit and any con doctor we can make any combinatorial logic gates circuit. It allows a very high speed at a very low cost all that without the use of semi-conductors.By combinatorial logic gates circuit we mean a circuit with distinct inputs and outputs (no outputs are forwarded back to the inputs).

Technical Problem

5. If agate in the set {‘XNOR’,‘XOR’} is verification and a gate in the set {‘NAND’,’NOR’} is implementation can we make implementation with verification only ?
Can we make implementation with wires only?

Solution to Problem

6. Evolution of the solution
- Step 1 :
Lets have 9 XORs and 3 distinct wires.0.0, 0.1 and 0.2 represent the 2 inputs and the output of the XOR number 0. pin0, pin1 and pin2 represent the 3 wires.First triple XOR:0.2, 1.0, 2.0 and the value 1 are connected together.1.2, 0.0, 2.1 and pin1 are connected together.2.2, 0.1, 1.1 and pin0 are connected together.Second triple XOR:3.2, 4.0, 5.0 and the value 1 are connected together4.2, 3.0, 5.1 and pin2 are connected together5.2, 3.1, 4.1 and pin0 are connected togetherThird triple XOR:6.2, 7.0, 8.0 and the value 1 are connected together7.2, 6.0, 8.1 and a changeable value 0 are connected together8.2, 6.1, 7.1 and pin0 are connected togetherA changeable value 0 is the value 0 separated with a resistance from the input output pin.A changeable value 1 is the value 1 separated with a resistance from the input output pin.If a pin fires back a different value the resistance would separate the 2 values. pin0 would be equal to pin1 NAND pin2.See figure 0.
- Step 2 :
How to obtain a not with wires only?Lets have two wires and flip them.Entering two different signals on a side of the two wires would have them reordered on the other side.
An order of the two values represents 0 and the other order represents 1. See figure 3.What can we obtain when we use wires instead of triple XORs?

Lets have 4 pins w0, w1, w2 and w3 and 3 wires linking w2 to w0, w2 to w1 and w2 to w3If w3 is put at 0 then w2 is approximating w0 AND w1All cases are drawn in figure 2.If w3 is put at 1 then w2 is approximating w0 OR w1All cases are drawn in figure 1.Figures 20 to 27 represent an electric version of the two functions.How to construct an approximation of universal gate with wires only?
Lets have :
- An OR with or0 = or1 OR or2;
- An AND with and0 = and1 AND and2; Where :
- input0, not(input0) are respectively connected to or1 , and1;-
input1, not(input1) are respectively connected to or2 , and2;-
and0, or0 are respectively connected to output, not(output)
“Notice flipping outputs to have a not”; As
- not(input0) AND not(input1) = input0 NOR input1 = output;
- not(output) = input0 OR input1;An approximation of universal NOR gate in constructed with wires only.
Figures 12,13,14 and 15 demonstrate the initial structure.
Figures 16 to 18 demonstrate replacing and approximating all with wires only. Flipping the gates it would become a NAND.
- Step 3:
How to remove the approximation? Lets have a wire with two switches on it.A sent signal on an end would not arrive to the other end unless the two buttons would allow it. The wire with the 2 buttons form an AND function without approximation.
Figure 4 to 7 demonstrate all cases of the described AND.
Lets have 2 pins linked with 2 distinct wires with a button each.A sent signal from a pin would not arrive to the other pin unless one of the buttons would allow it.
The 2 wires with the 2 buttons form an OR function without approximation. Figure 8 to 11 demonstrate all cases of the described OR.
Lets have 2 parallel wires intersecting with another 2 parallel wires.A signal is sent in one of the first 2 and a signal is sent on

one of the second 2. If the bottom on the buttons side connects 2 parallel wires the top on the other side would have the signal on both wires.If the top on the buttons side connects 2 parallel wires the bottom right on the other side would have the signal on both wires.The 4 wires with the 2 buttons form a function not without approximation. See Figure 51How to construct a universal gate with wires only?
Lets have 8 pins from 0 to 7 in the inputs. Lets have 4 pins from 8 to 11 in the outputs.0 - 4 - 10 are connected together as group 1.1 - 5 - 11 are connected together as group 2.2 - 8 are connected together as group 3.3 - 6 are connected together as group 4.7 - 9 are connected together as group 5.A switch connects pin 0 with pin 1 at a position and pin 2 with pin 3 at the other
A switch connects pin 4 with pin 5 at a position and pin 6 with pin 7 at the other A switch is always at one of the 2 positions but not at both.A signal is sent through pin 8 or through pin 9 but not through both.A signal is sent through pin 10 or through pin 11 but not through both.
Only one of the 2 signals would come back (only one of the pins 8 - 9 - 10 -11 would have no signal).Unless both switches are at the second position (at a 0) only one of the pins 8-9 would have a signal (the result would be a 0). It is a NOR.
If we flip the encoding having a zero at the smaller pins ids then Unless both switches are at the second position (at a 1) only one of the pins 8-9 would have a signal (the result would be a 1). It is a NAND.Figure 29 to 33 are frames of a movie demonstrating the propagation of signals when both switches are up.Figure 34 to 38 are frames of a movie demonstrating the propagation of signals when the upper switch is down and the bottom switch is up.Figure 39 to 43 are frames of a movie demonstrating the propagation of signals when the upper switch is up and the bottom switch is down.Figure 44 to 50 are frames of a movie demonstrating the propagation of signals when both switches are down.Some groups of pins may be at void.A void is

a signal that is replaced by a value when coexisting with it.

Advantageous Effects of Invention

7. A signal could be some characteristics of a light like color, frequency or temperature, of an electric current or voltage, of a gas like sound or pressure, of a solid like sand, smoke or smell and finally of a liquid like taste or fluidity.It does not require semi conductors or any kind of inner circuit switching (it does

not require transistors).And there for the materialization of logic and programs could extend its domain out of electricity.

Brief Description of Drawings

8. [Fig.0] How to make a NAND with XORS
[Fig.1] An approximation of an OR with wires
[Fig.2] An approximation of an AND with wires
[Fig.3] A NOT with wires only
[Fig.4 to fig.7] Demonstration of all the cases of an approximation-less AND
[Fig.8 to fig.11] Demonstration of all the cases of an approximation-less OR
[Fig.12 to fig.15] Demonstration of all the cases of an approximation-less Universal gate using an OR and an AND
[Fig.16 to fig.19] Demonstration of all the cases of an approximation of a Universal gate using wires only
[Fig.20 to fig.23] An electric approximation of an AND with wires
[Fig.24 to fig.27] An electric approximation of an OR with wires
[Fig.28] Used Symbols descriptions (the bottom two descriptions do apply for figures 29 to 50)
[Fig. 29 to 33] are frames of a movie demonstrating the propagation of signals when both switches are up.
[Fig. 34 to 38] are frames of a movie demonstrating the propagation of signals when the upper switch is down and the bottom switch is up.

[Fig. 39 to 43] are frames of a movie demonstrating the propagation of signals when the upper switch is up and the bottom switch is down.
[Fig. 44 to 50] are frames of a movie demonstrating the propagation of signals when both switches are down.
[Fig. 51] Approximation-less, universal gate construction demonstration.
[Fig. 52] An example of a memory circuit using some kind of commanded switches like transistors or relays.
[Fig. 53 to fig. 56] Use of the technology to make a small adder.

Description of Embodiments

9. By combinatorial logic gates circuit we mean a circuit with distinct inputs and outputs (no outputs are forwarded back to the inputs). A combinational logic circuit structure is included in a circuit that forwards back the outputs to the inputs. A circuit usually forwards back the outputs to the inputs for memory purposes. See figure 52.The apparatus described as a combinational logic circuit structure is made with buttons and pins. A button has 4 pins and two possible positions, connecting two of them at a position and the other two at the other position. There are pins at the inputs with buttons and pins at the outputs, if we remove the buttons we can notice that pins are connected forming groups, where a value change to one pin in a group, is a value change to all pins in the group. The embodiment of the described apparatus do not require a specific size like nanometers or kilometers or a specific material other then a material that can keep a group of pins connected given the chosen signal whether that is some characteristics of a light like color, frequency or temperature, of an electric current or voltage, of a gas like sound or pressure, of a solid like sand, smoke or smell and finally of a liquid like taste or fluidity.

Examples

10. [Fig. 52] An example of a memory circuit using some kind of commanded switches like transistors or relays to make an alarm system that would not shut the siren if the siren is ON and the door is re-closed.
[Fig. 53 to fig. 56] Use of the technology to make a small adder with some examples like 11+11=110.

Industrial Applicability

11. It is highly relevant to chips manufacturers.

Claims

1 - A combinational logic circuit structure consisting of: one or more inputs which are one or more pins,one or more outputs which are one or more pins, wherein the pins are subdivided into groups,

wherein a value of a binary digit or of a void is determined by characteristics, of a light, of an electric signal, of a gas or of a liquid or of a solid and assigned to a pin,wherein a value change to one pin in a group is a value change to all pins in the group, wherein groups are connected to each other with input switches,

and wherein groups are disconnected from each other with the said input switches.

2 - A combinational logic circuit structure process consisting of the steps of:Providing connected groups of one or more pins;Providing a value of a binary digit or of a void determined by characteristics of a light, of an electric signal, of a gas or of a liquid or of a solid and assigned to a pin;Providing some groups put at binary value and some groups put at void;Providing switches configured to connect and disconnect some groups;Wherein said switches decide the value of some groups.

Abstract

- Before this work: The field of computer engineering was about the use of (‘NAND’, ’NOR’) as universal logic gates to make processors and materialize programs. Some of the field of electric engineering was about realizing those universal gates using transistors. Some of the field of chemical engineering was about using rare earth mines as semi conductors to make those transistors.

- After this work: Conductors would permit to replace semi-conductors for the manufacturing of memoryless parts of chips.

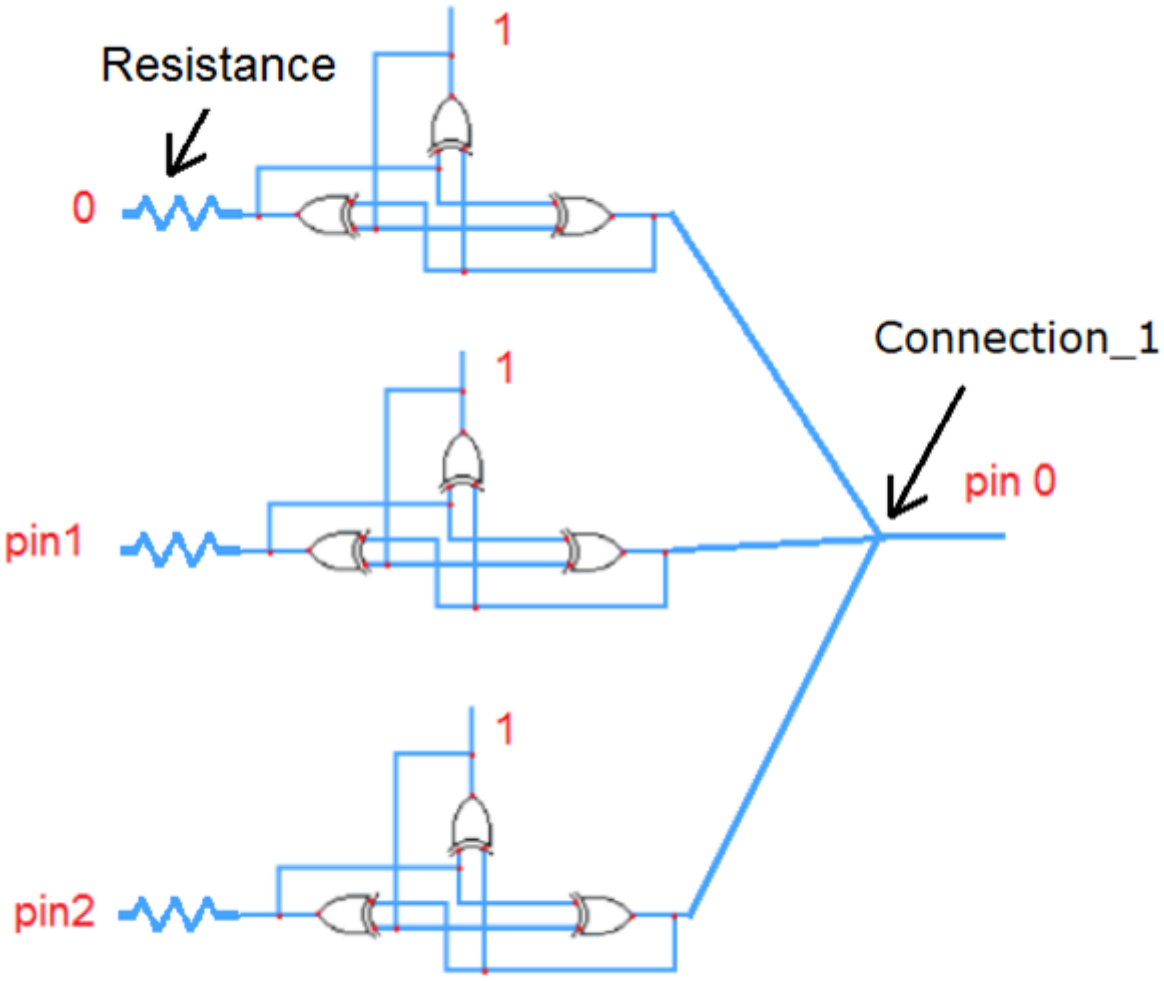
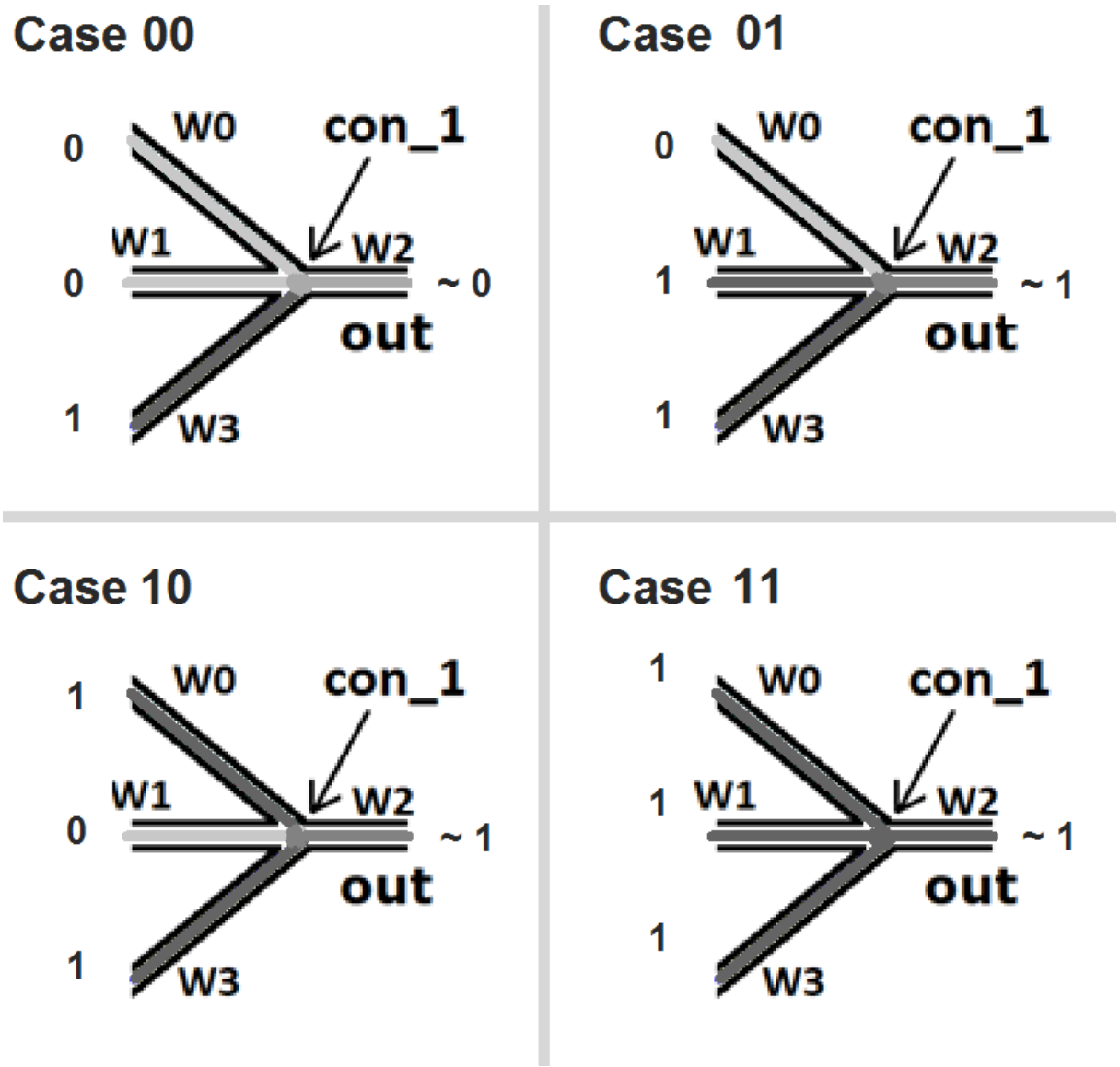


Fig.0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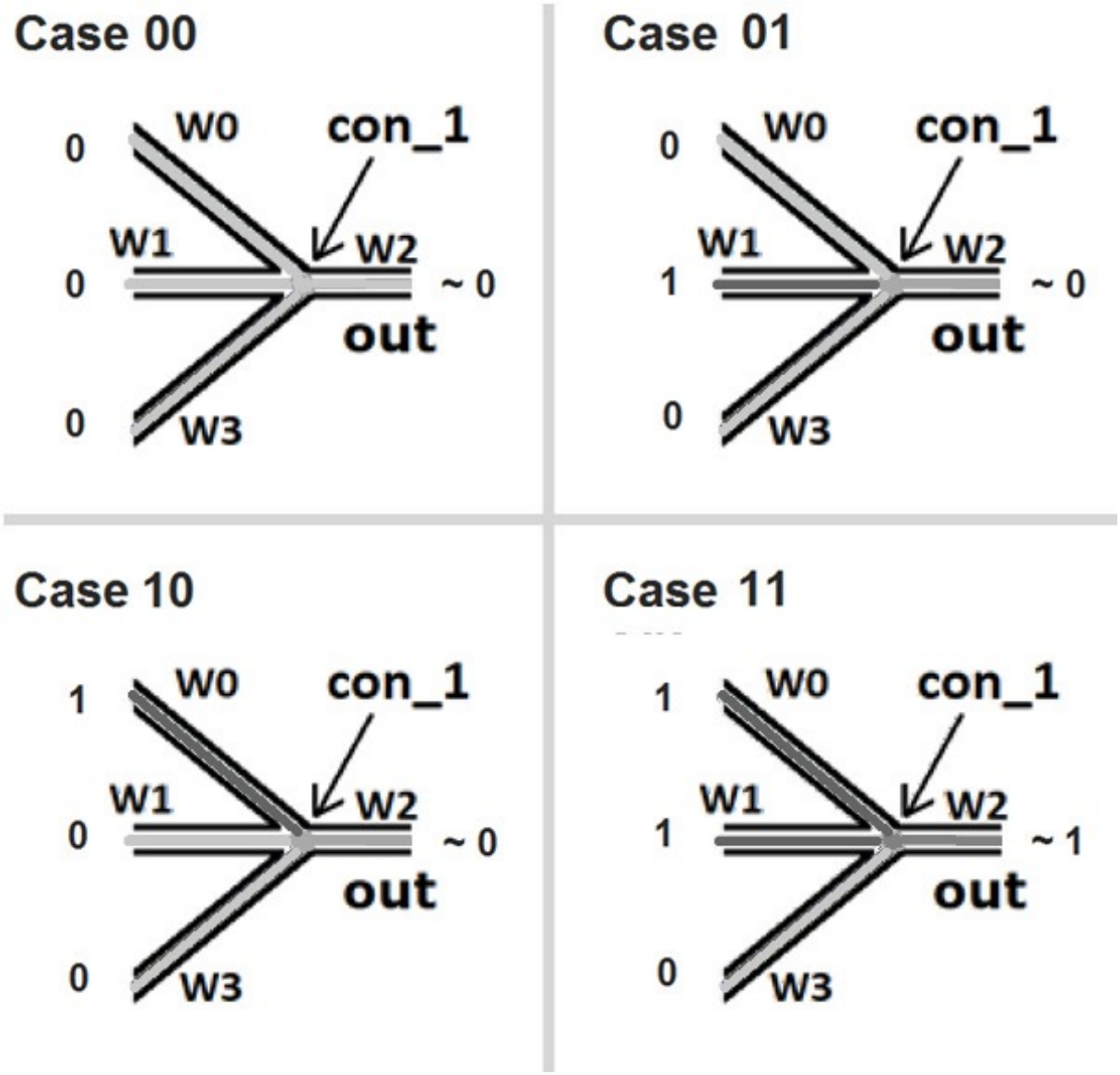
W1
W2
0
~ 0
out
1
W3
Case 01
0
W0
con_1
W1
W2
1
~ 1
out
1
W3
Case 10
1
W0
con_1
W1
W2
0
~ 1
out
1
W3
Case 11
1
W0
con_1
1
W1
W2
~ 1
out
1
W3

Fig.1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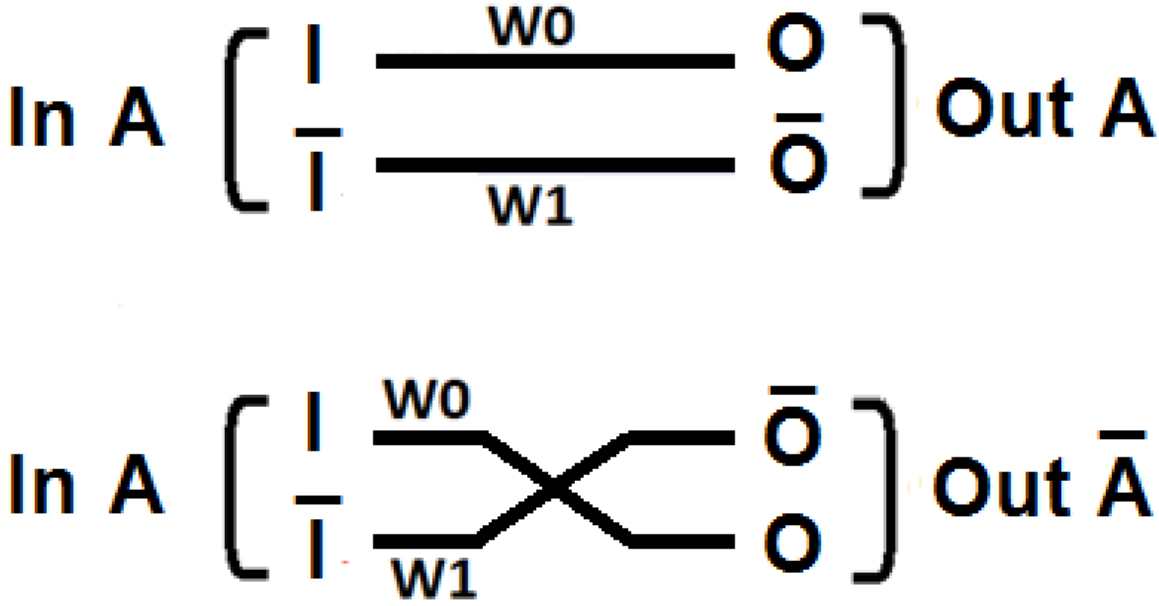
W0
con_1
W1
W2
0
~ 0
out
0
W3
Case 01
0
W0
con_1
W1
W2
1
~ 0
out
0
W3
Case 10
1
W0
con_1
W1
W2
0
~ 0
out
0
W3
Case 11
1
W0
con_1
W1
W2
1
~ 1
out
0
W3

Fig.2



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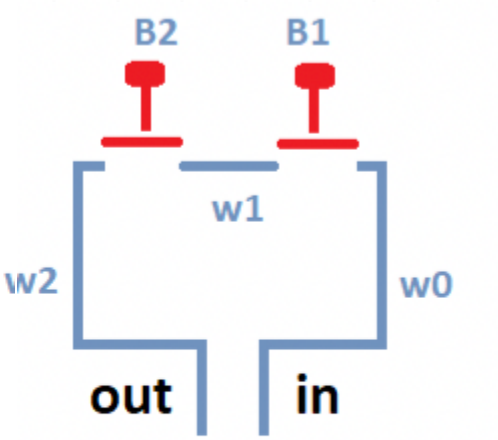
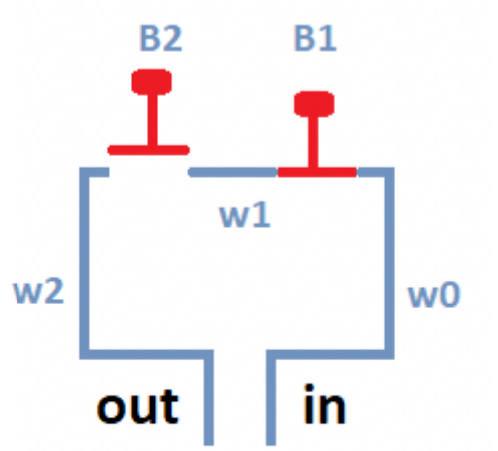


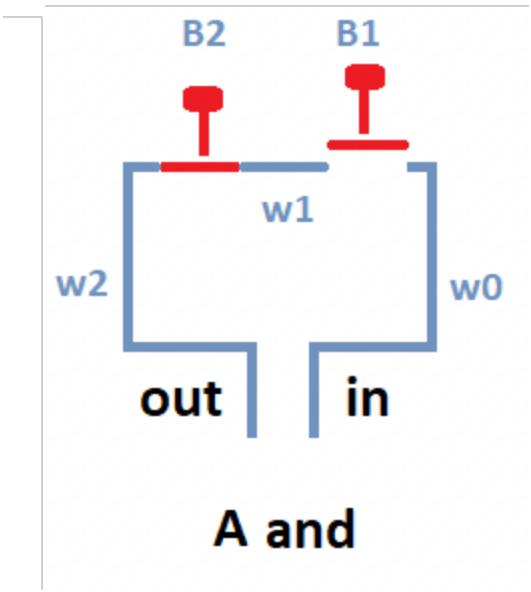
A and

Fig.4



A and

Fig.5



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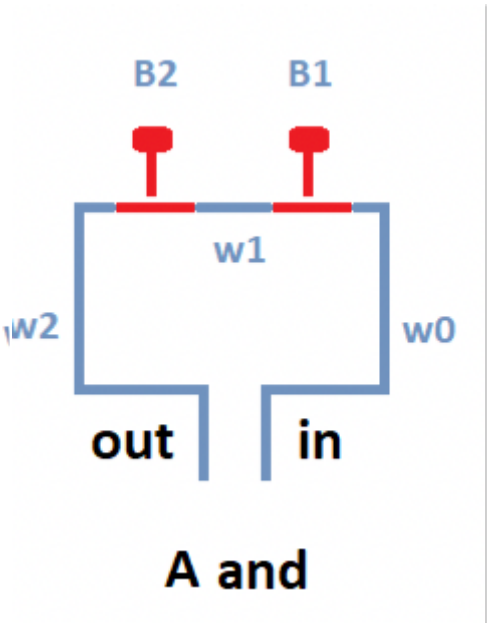

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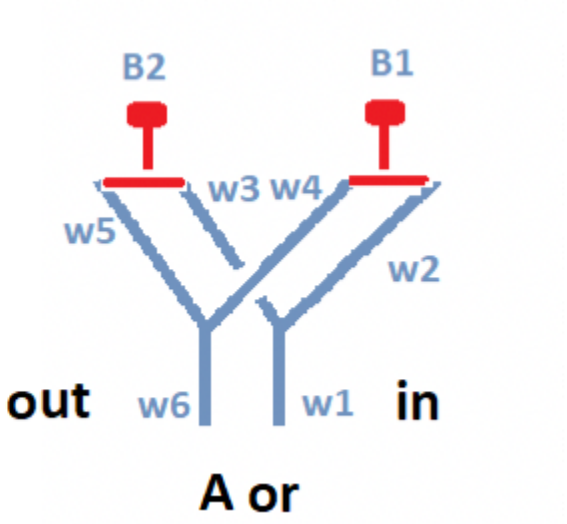
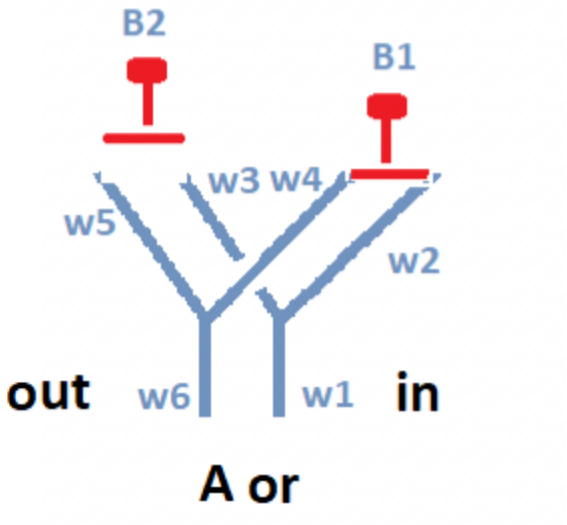


A or

Fig.8



A or

Fig.9

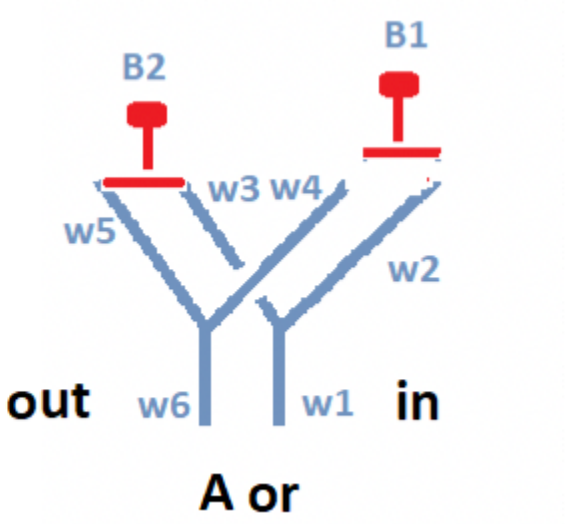
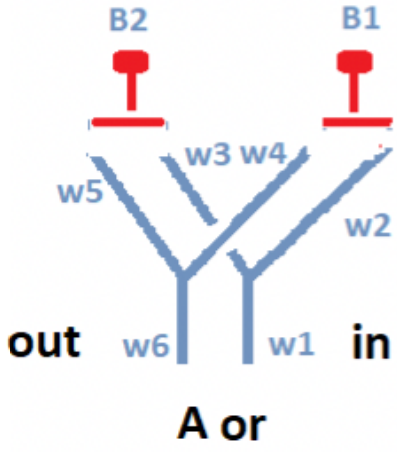


Fig.10



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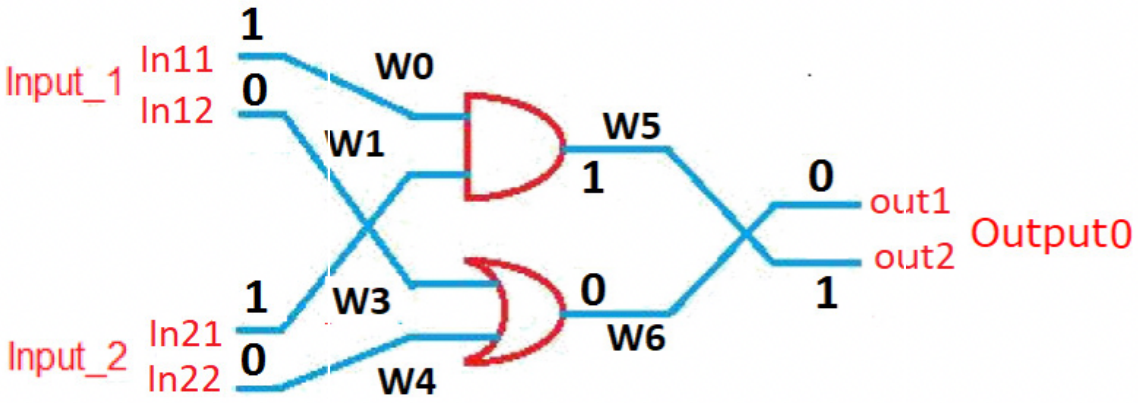
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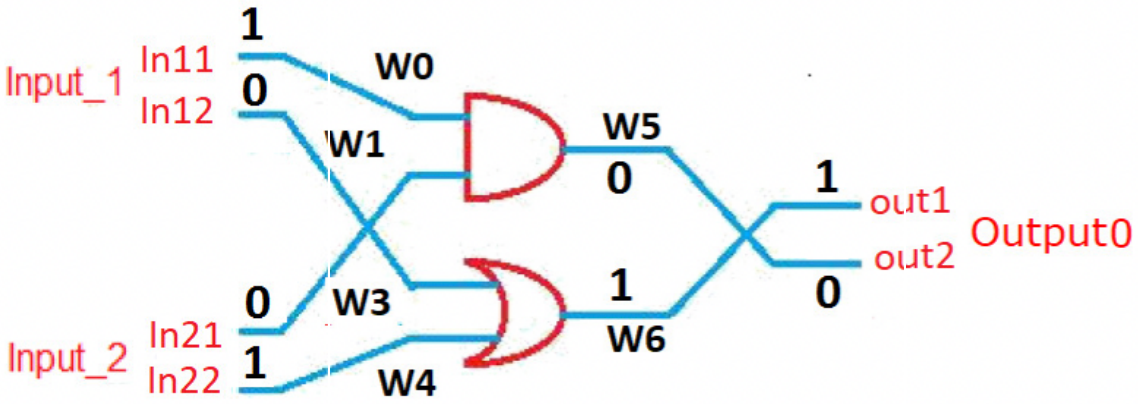
In12
1
0
W0
W1
W5
1
0
out1
out2
Output0
1
W3
0
W6
1
Input_2
In21
In22
0
W4

Fig.12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In12
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0
W0
W1
W5
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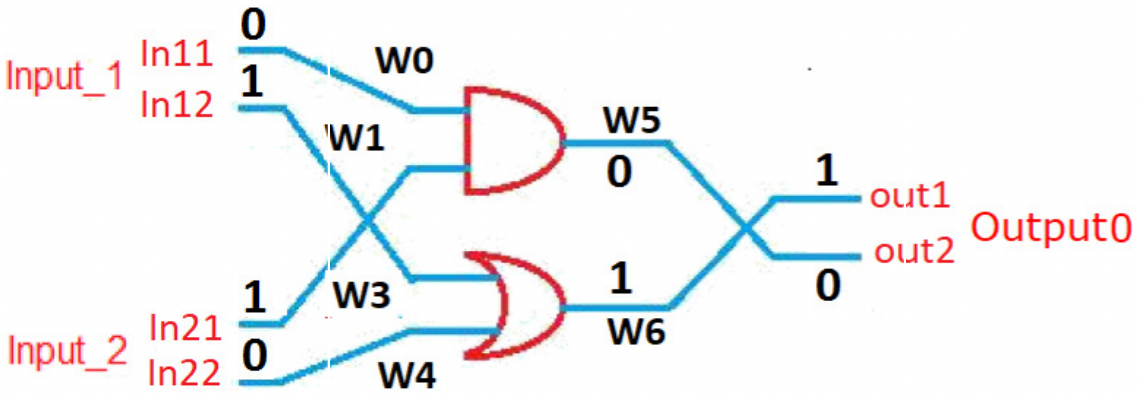
1
out1
out2
Output0
0
W3
1
W6
0
Input_2
In21
In22
1
W4

Fig.13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In12
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1
W0
W1
W5
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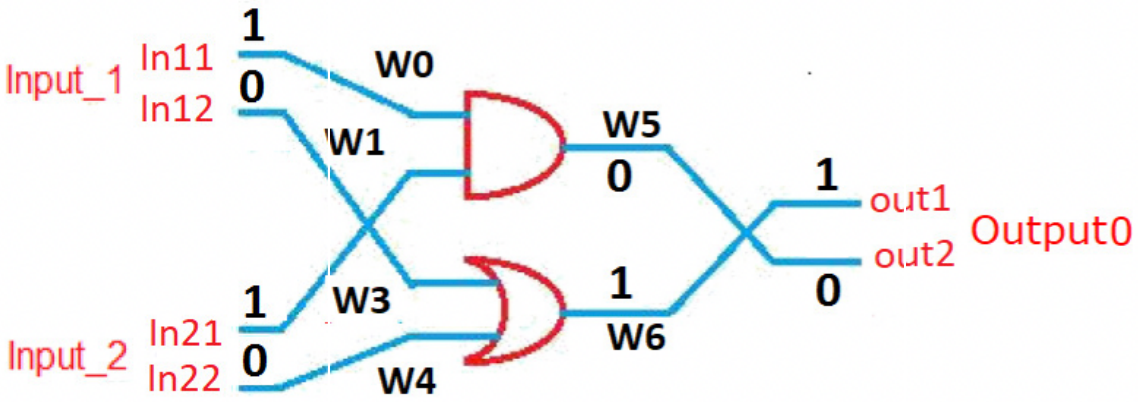
1
out1
out2
Output0
0
Input_2
In21
In22
1
0
W3
W4
1
W6

Fig.14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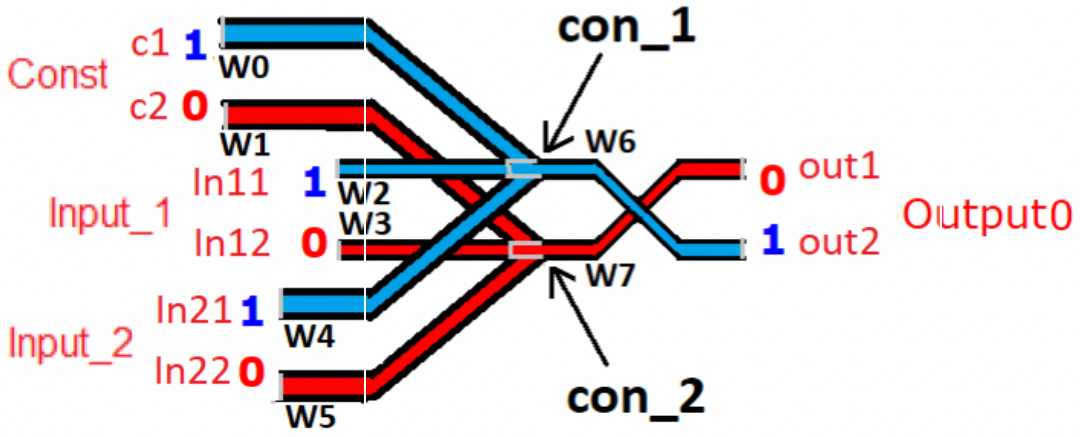
In22
1
0
W3
W4
1
W6

Fig.15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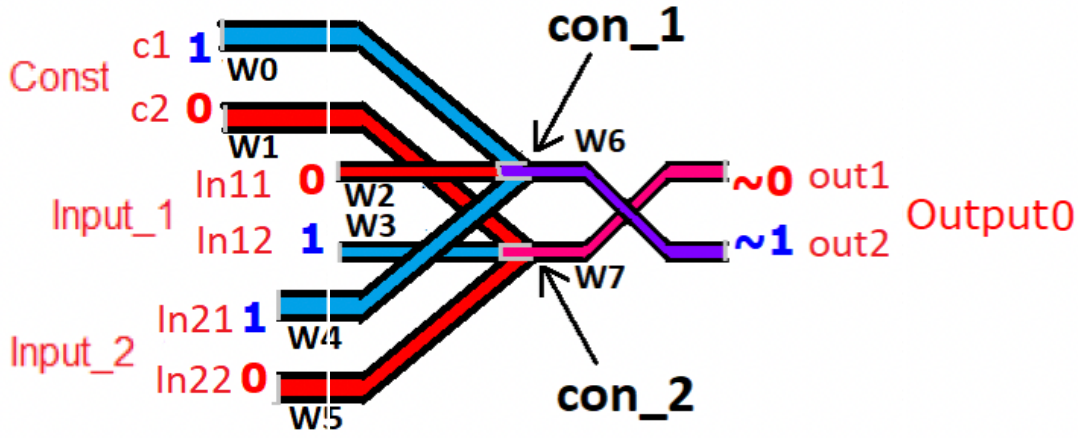
W0
c2 0
W1
Input_1
In11 1
W2
W3
In12 0
Input_2
In21 1
W4
In22 0
W5
con_1
W6
W7
con_2
0 out1
1 out2
Output0

Fig.16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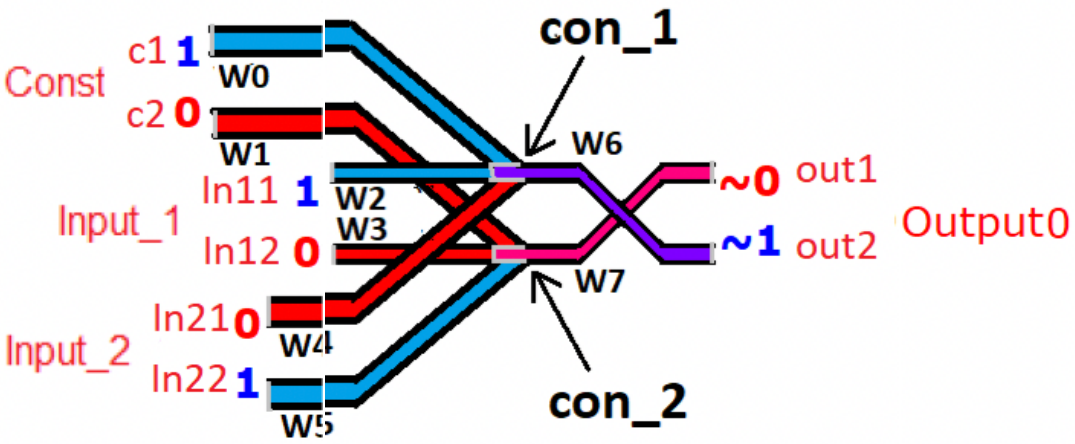
W0
c2 0
W1
Input_1
In11 0
W2
W3
In12 1
Input_2
In21 1
W4
In22 0
W5
con_1
W6
W7
con_2
~0 out1
~1 out2
Output0

Fig.17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W0
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W1
W6
In11 1
W2
~0 out1
Input_1
W3
Output0
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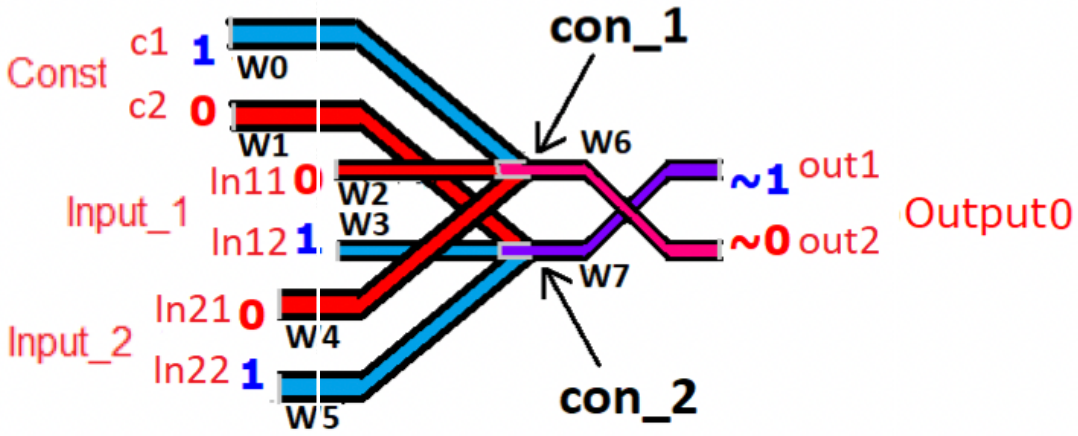
W7
In21 0
W4
Input_2
In22 1
W5
con_2

Fig.18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c2 0
W1
W6
In11 0
W2
~1 out1
Input_1
W3
Output0
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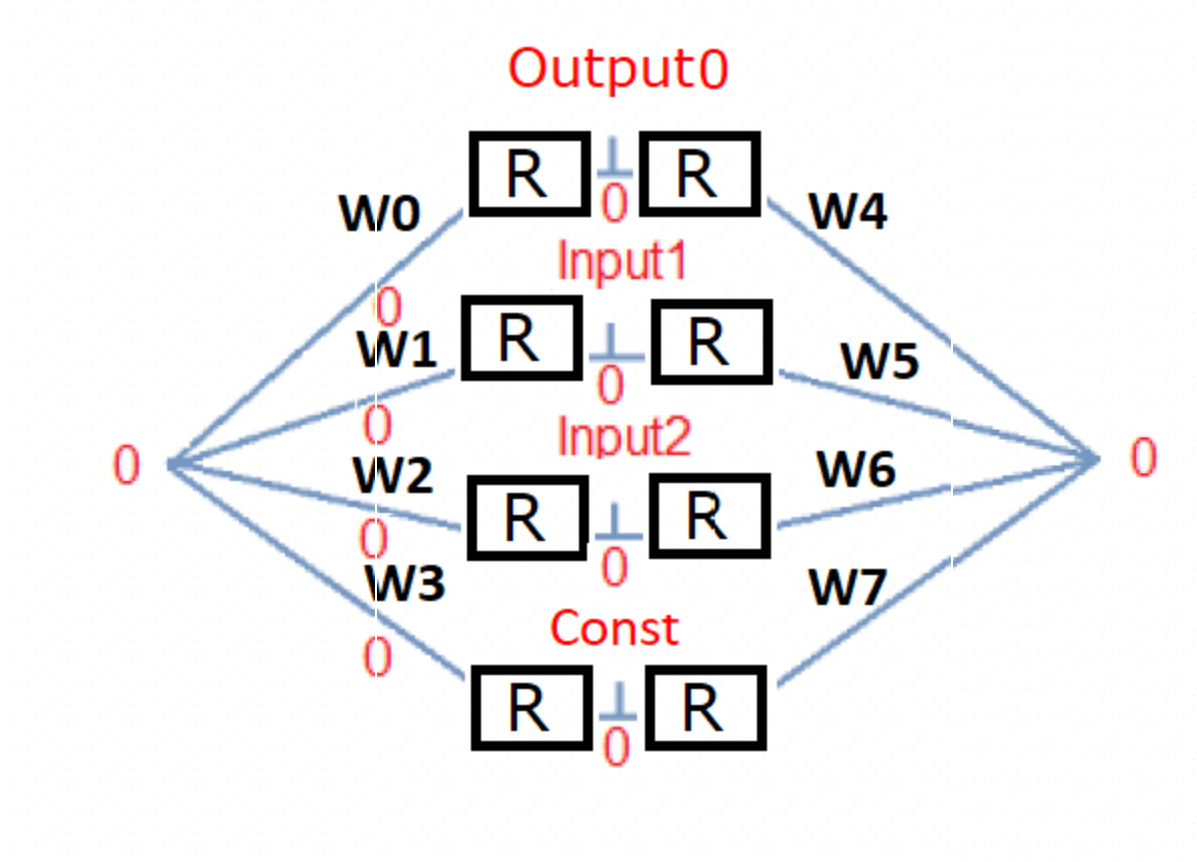
~0 out2
W7
In21 0
W4
Input_2
In22 1
W5
con_2

Fig.19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R
0
W0
W4
Input1
0
W1
R
R
0
W5
0
Input2
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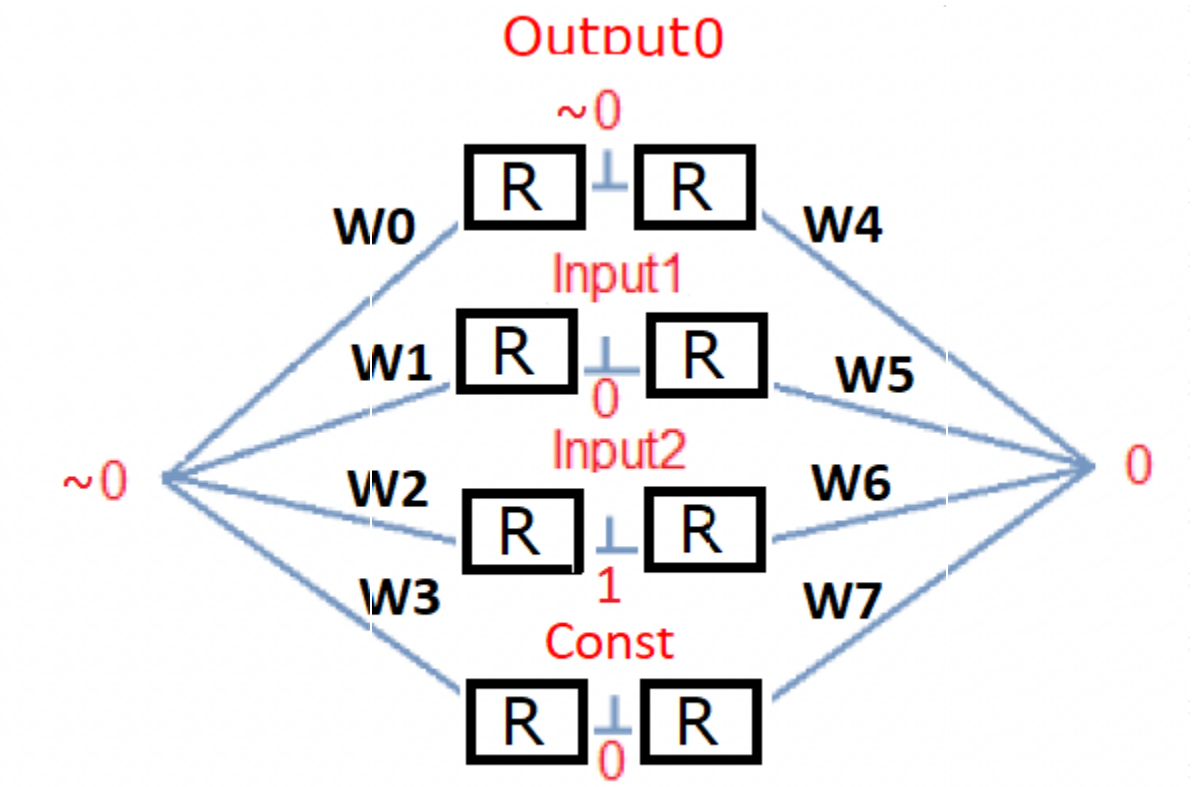
W2
W6
R
R
0
0
0
W3
W7
Const
0
R
R
0

Fig.20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W0
W4
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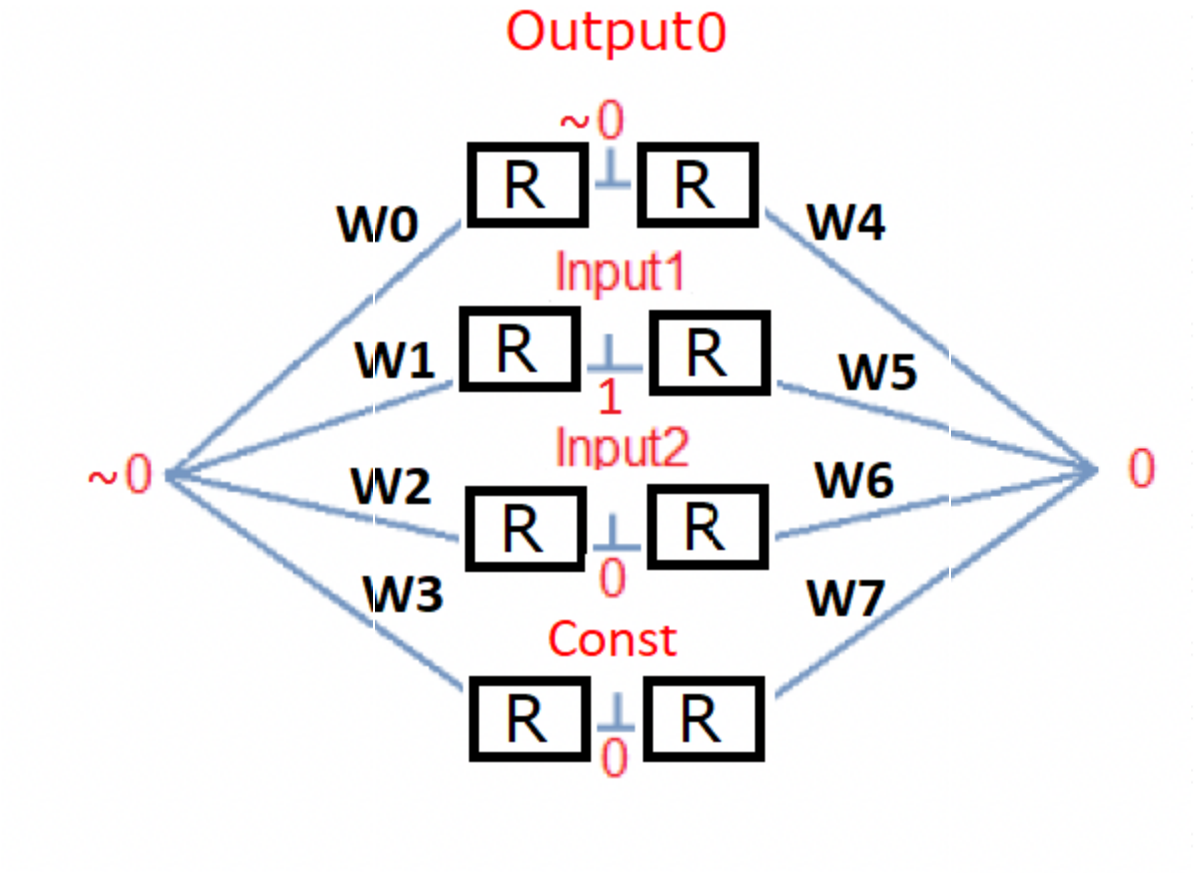
1
W3
W7
Const
R
R
0

Fig.21


Output0
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R
R
W0
W4
Input1
W1
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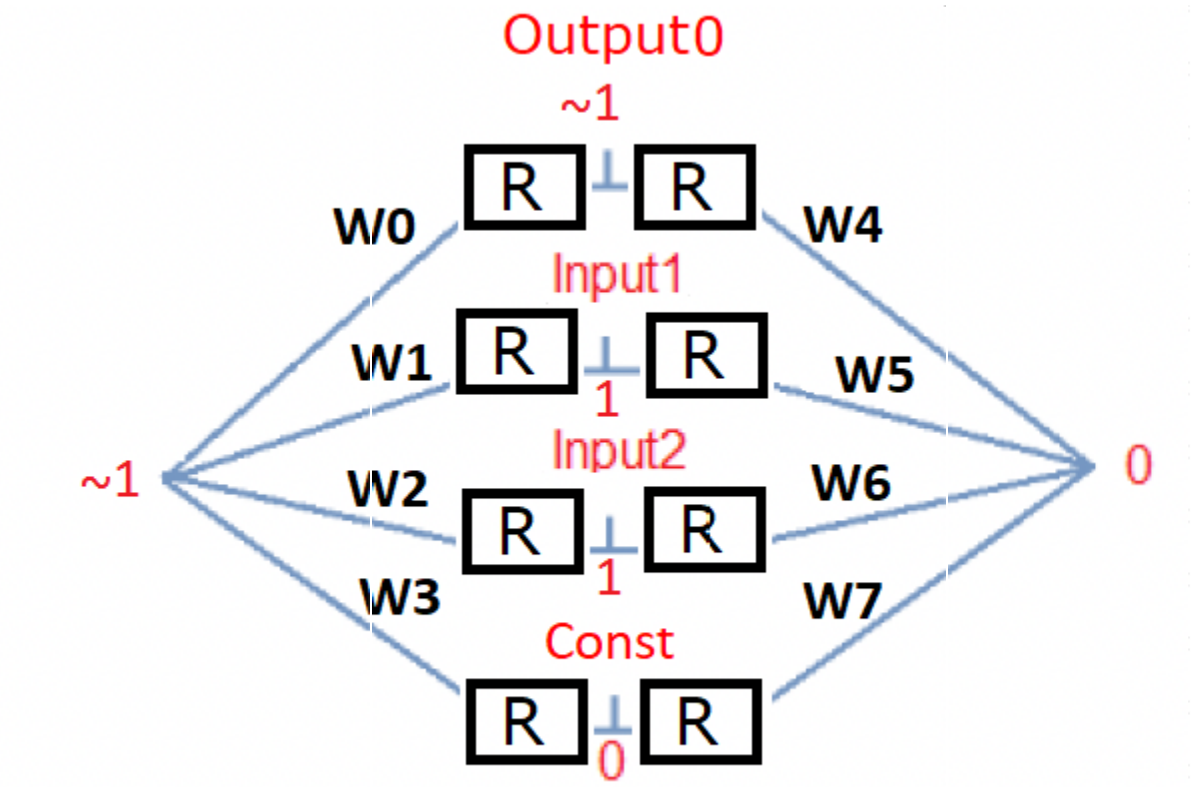
R
W3
W7
0
Const
R
R
0

Fig22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R
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W4
Input1
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Input2
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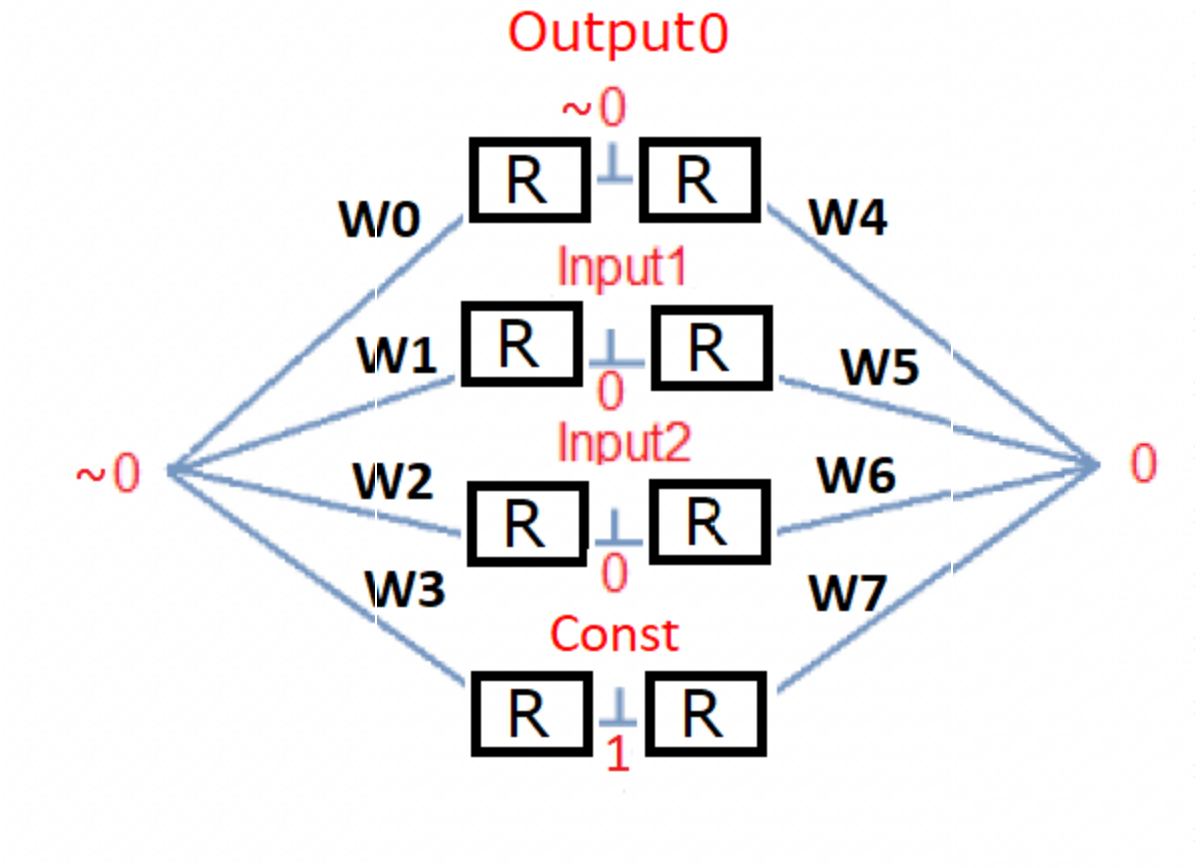
1
W3
W7
Const
R
R
0

Fig.23


Output0
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R
R
W0
W4
Input1
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R
W5
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Input2
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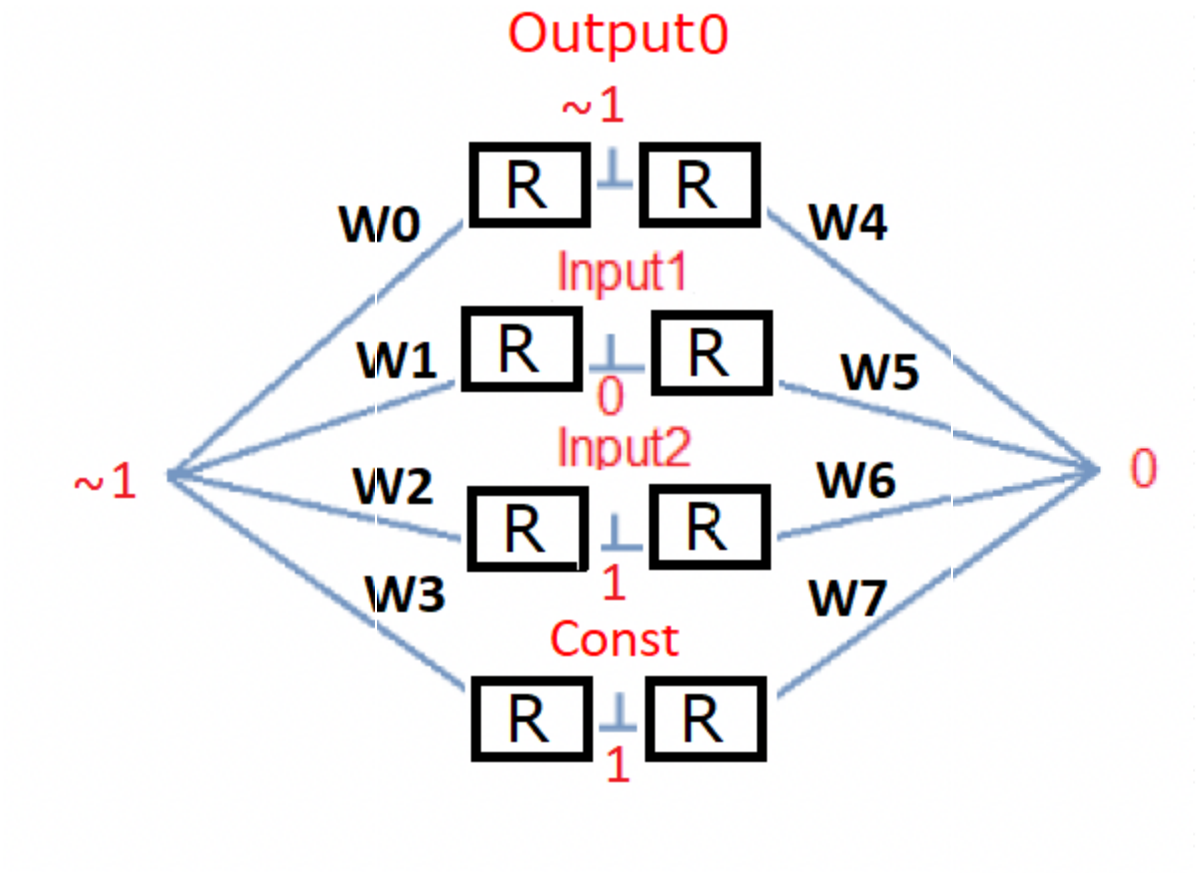
R
R
W3
W7
0
Const
R
R
1

Fig.24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W4
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W5
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Input2
~1
W2
W6
0
R
R
W3
1
W7
Const
R
R
1

Fig.25

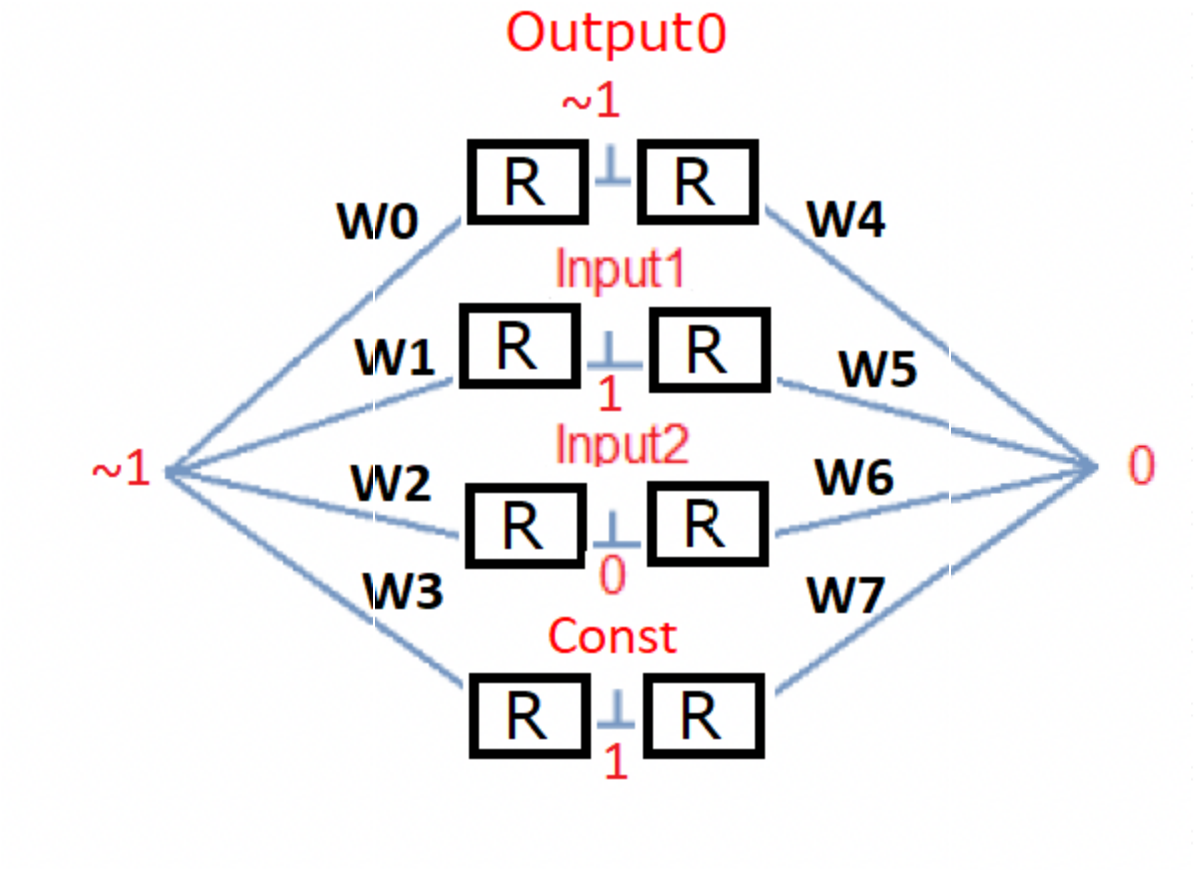

Output0
~1
R
R
W0
W4
Input1
W1
R
R
W5
1
~1
Input2
0
W2
W6
R
R
0
W3
W7
Const
R
R
1

Fig.26

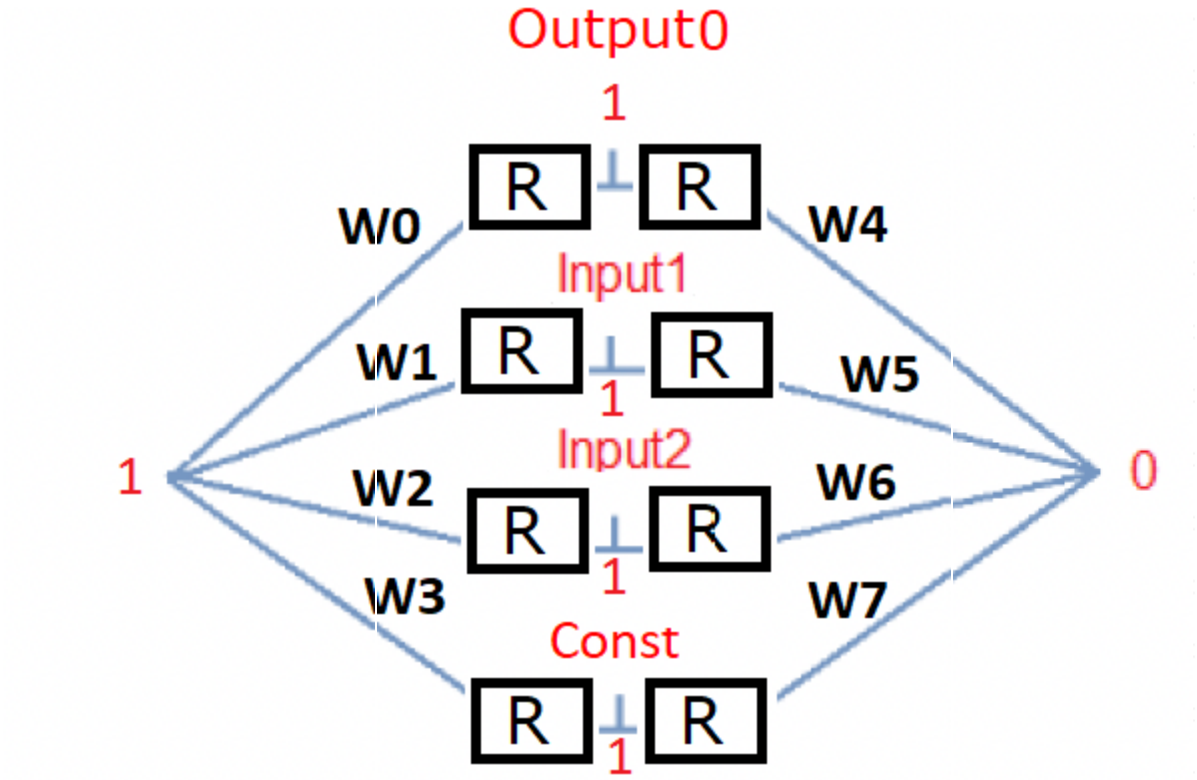

Output0
1
R
R
W0
W4
Input1
W1
R
R
W5
1
Input2
1
W2
W6
0
R
R
W3
1
W7
Const
R
R
1

Fig.27

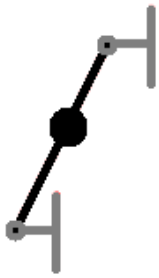
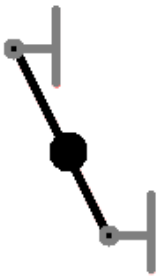
■	is a pin
1	is a connected group of pins
2, 3, 4, 5	are also groups of pins
	a button at a state connecting the top two pins
	a button at a state connecting the bottom two pins
1, 2	are groups that form an OR
3, 4, 5	are groups that form an AND

Fig.28

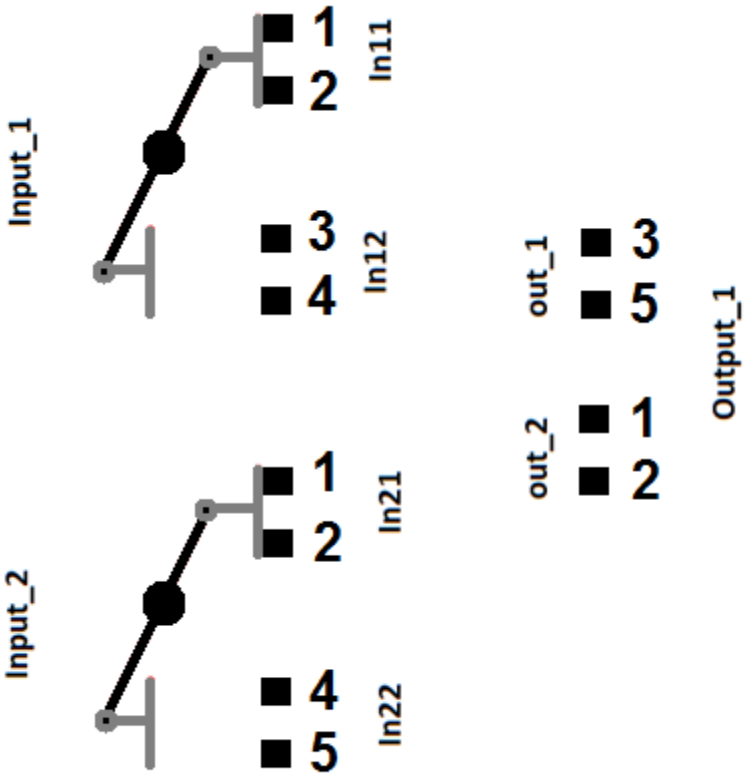

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.29

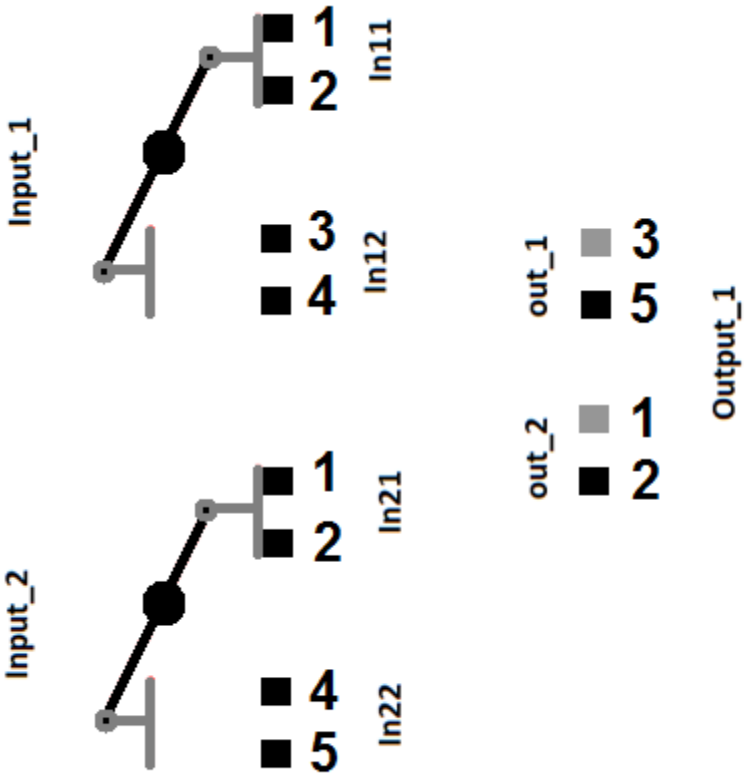

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.30

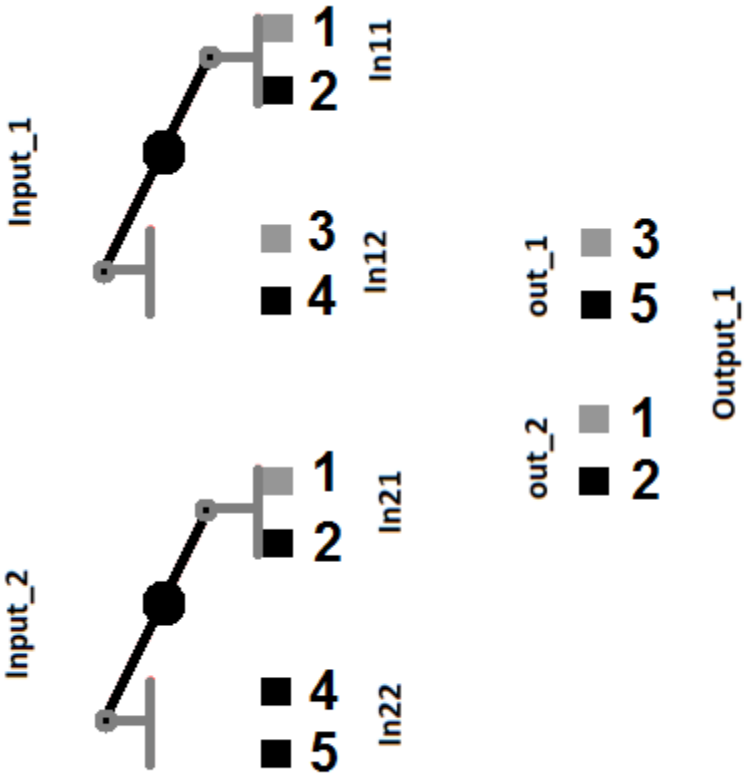

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.31

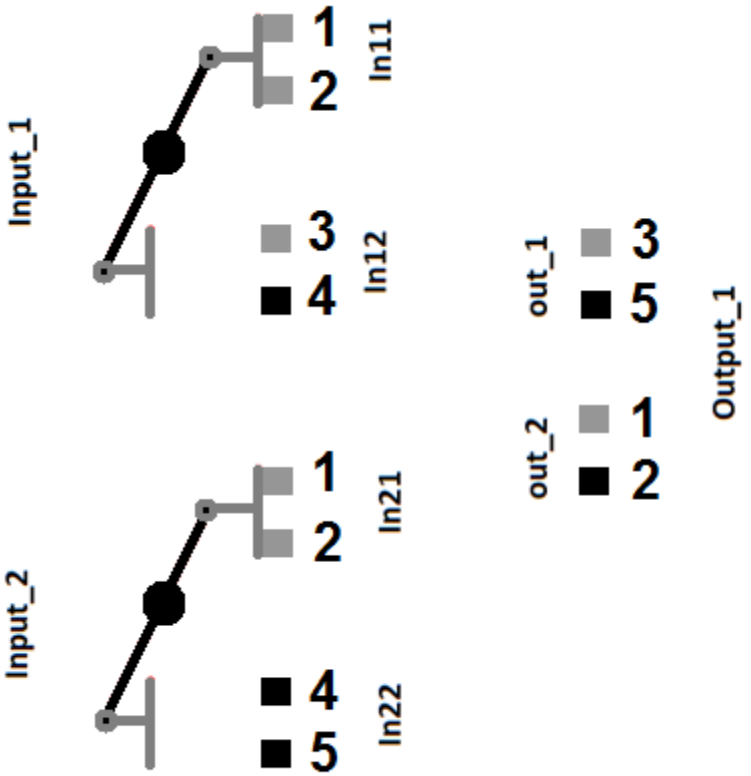

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.32

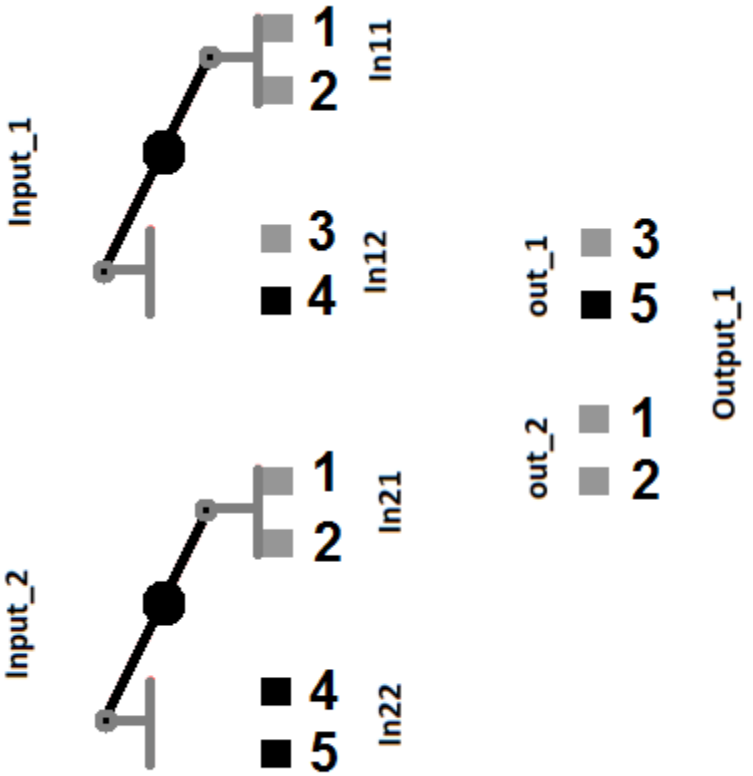

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.33

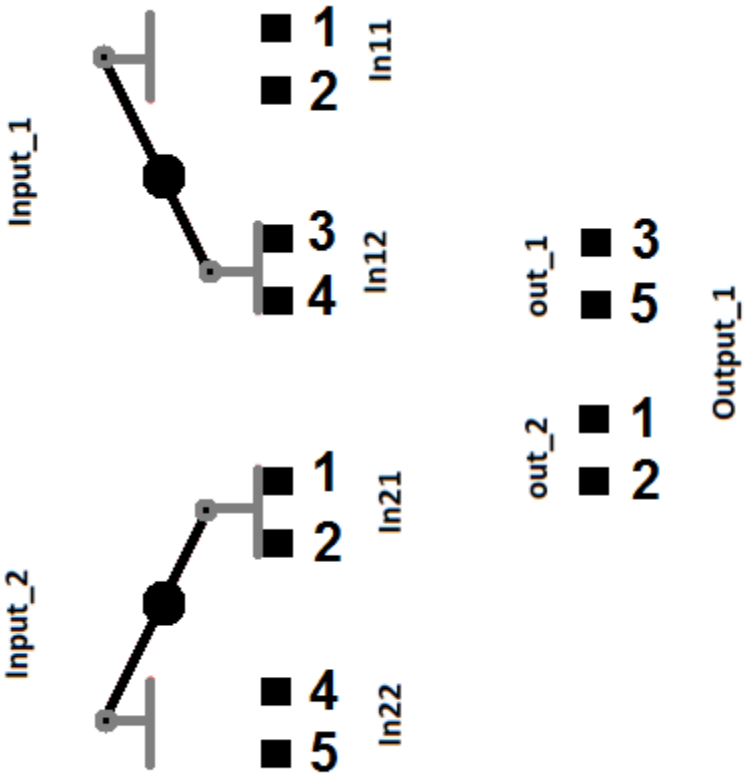

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.34

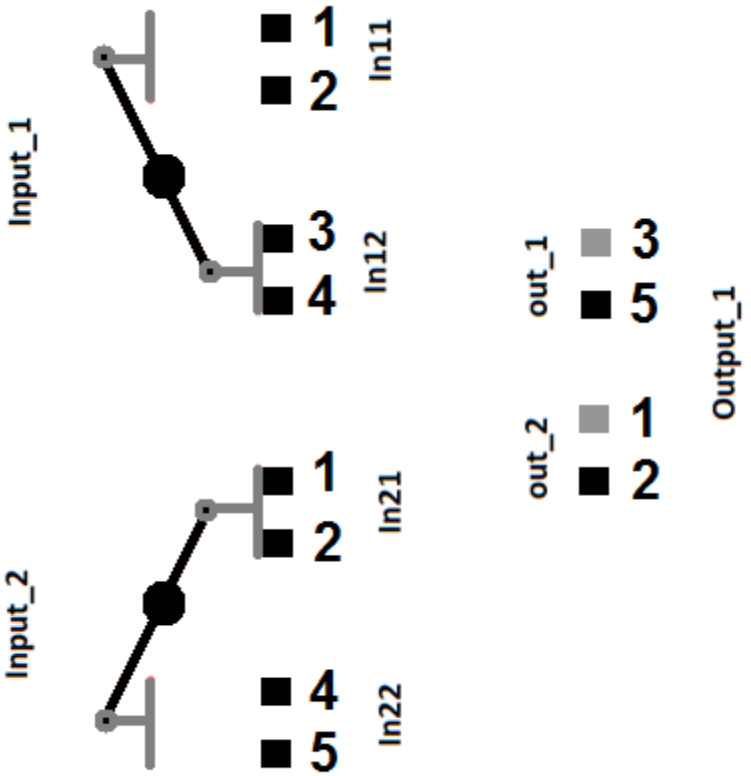

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.35

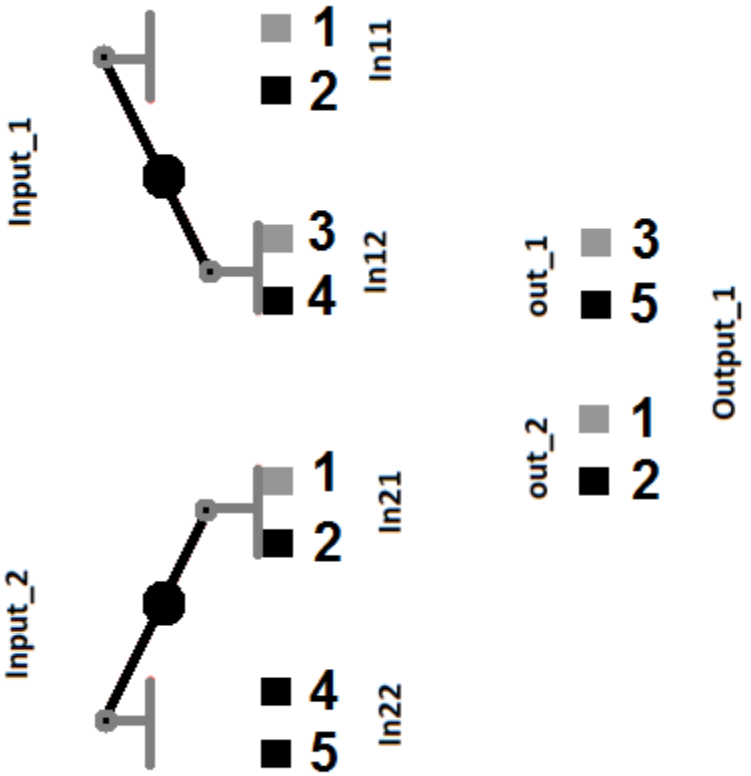

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.36

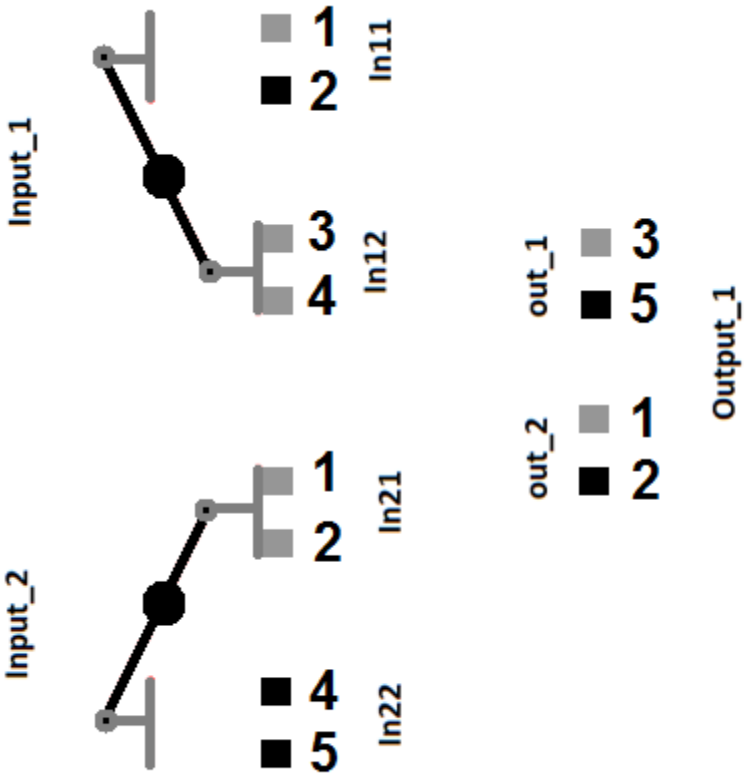

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.37

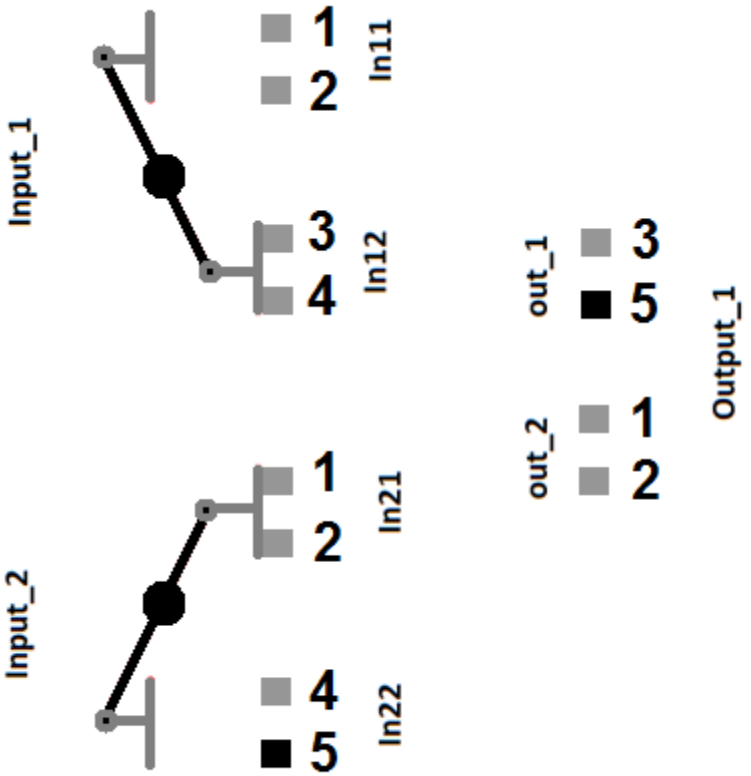

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.38

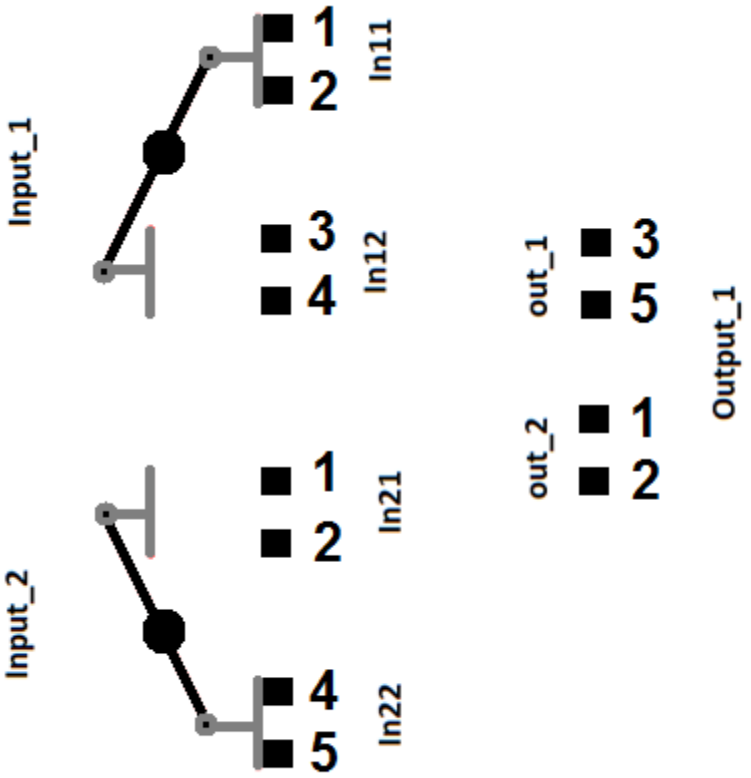

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.39

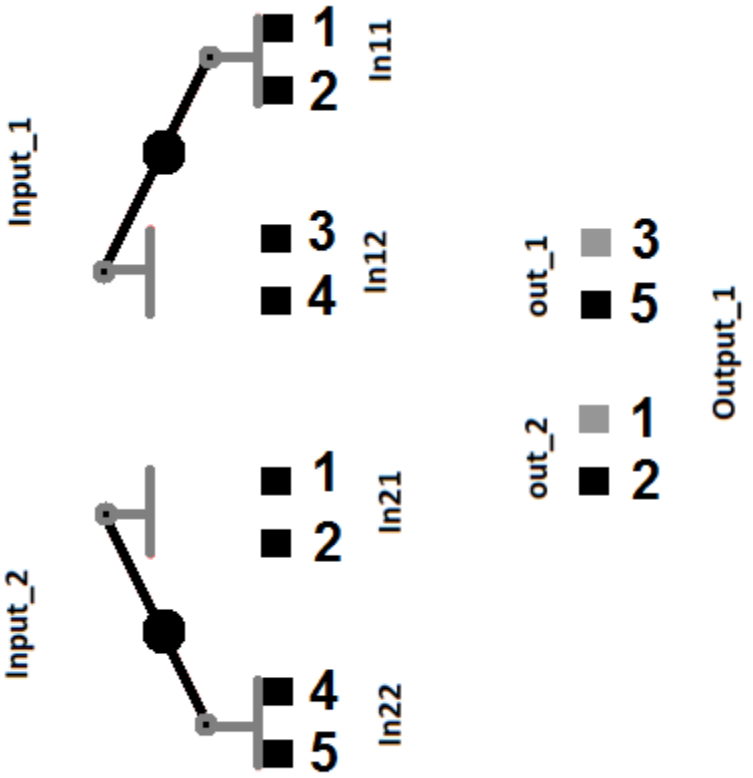

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.40

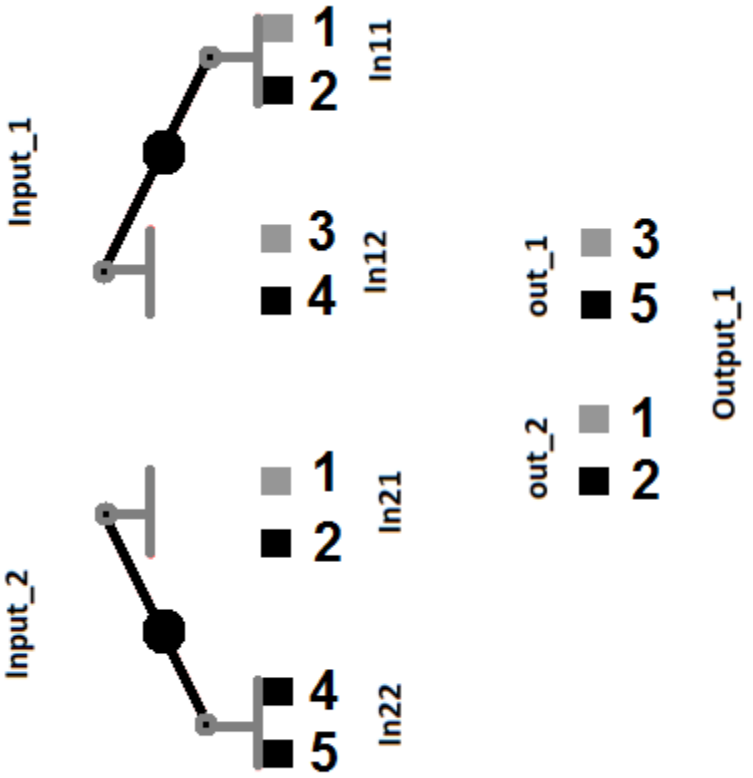

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.41

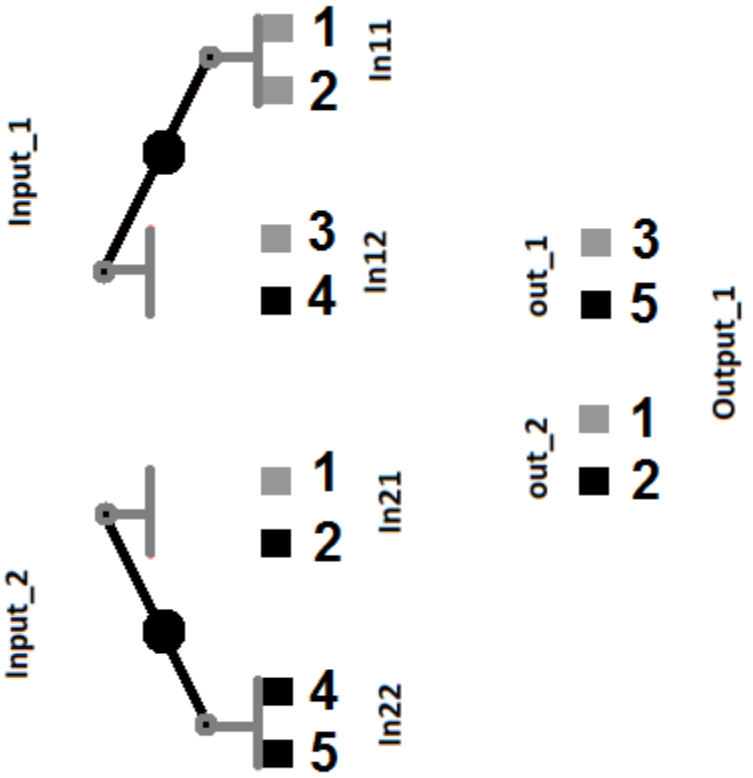

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.42

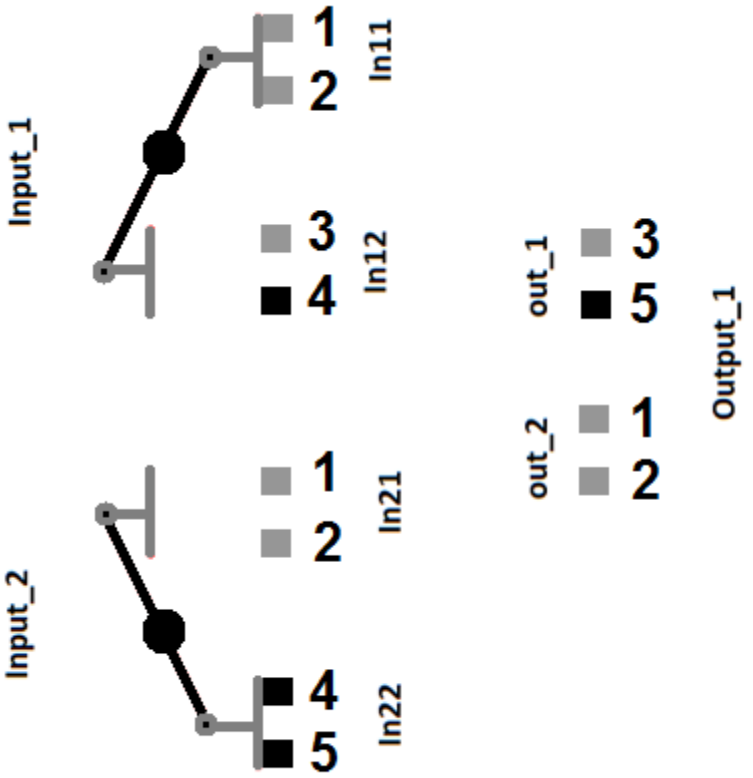

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.43

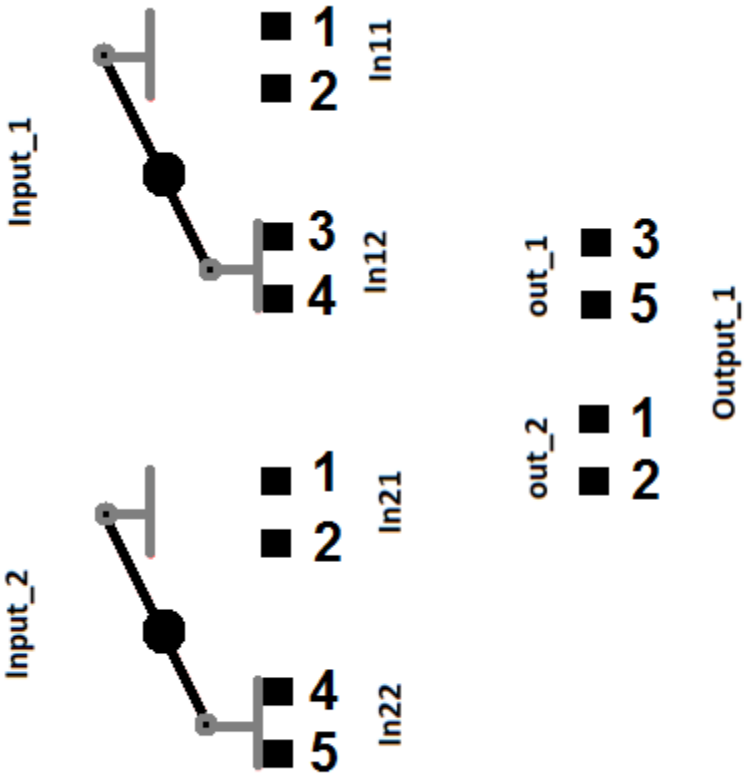

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.44

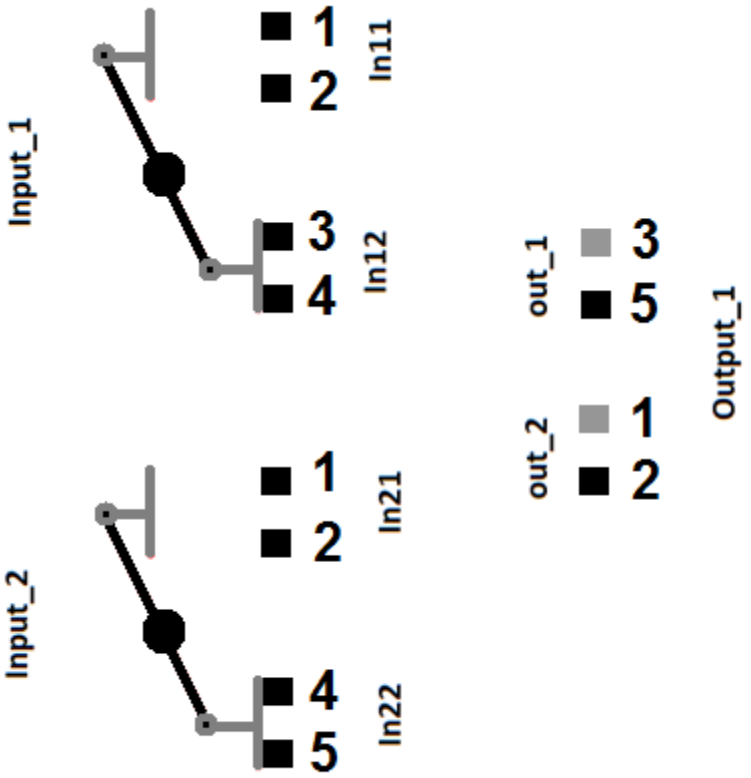

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.45

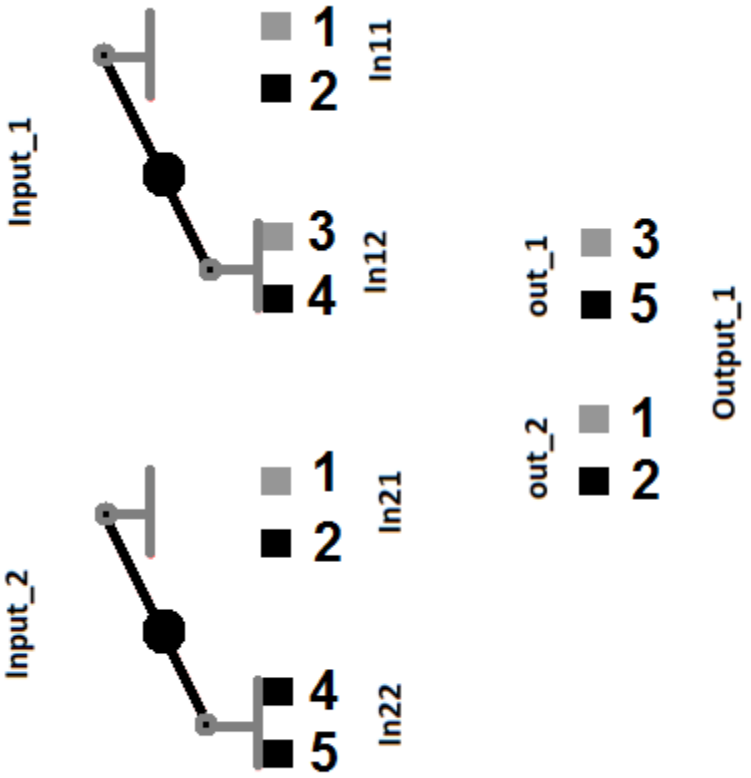

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.46

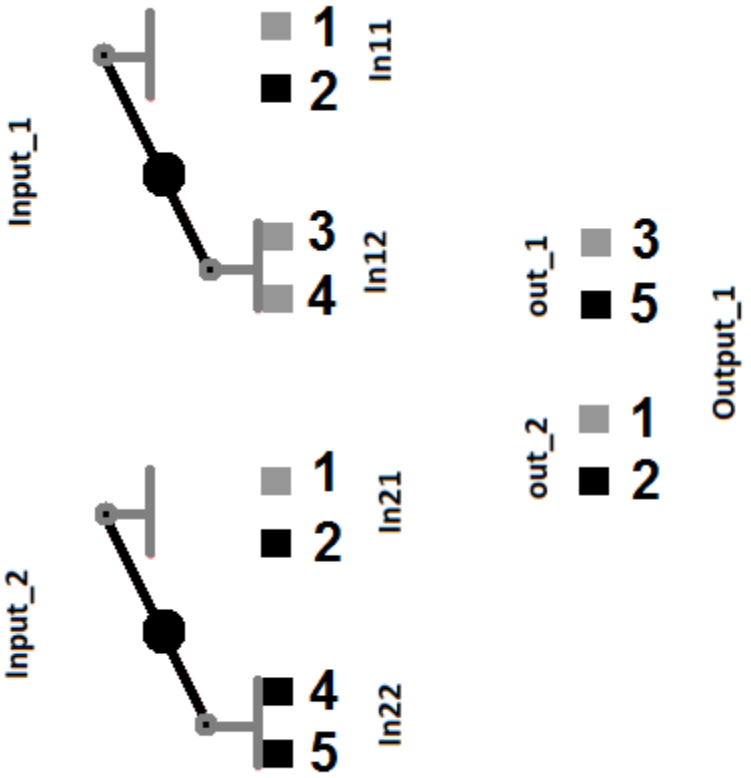

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.47

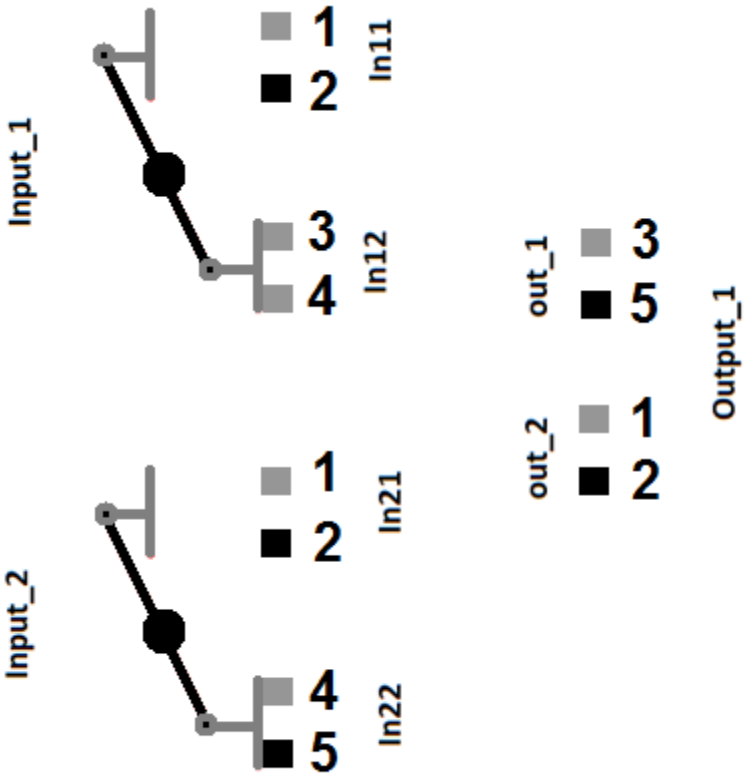

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.48

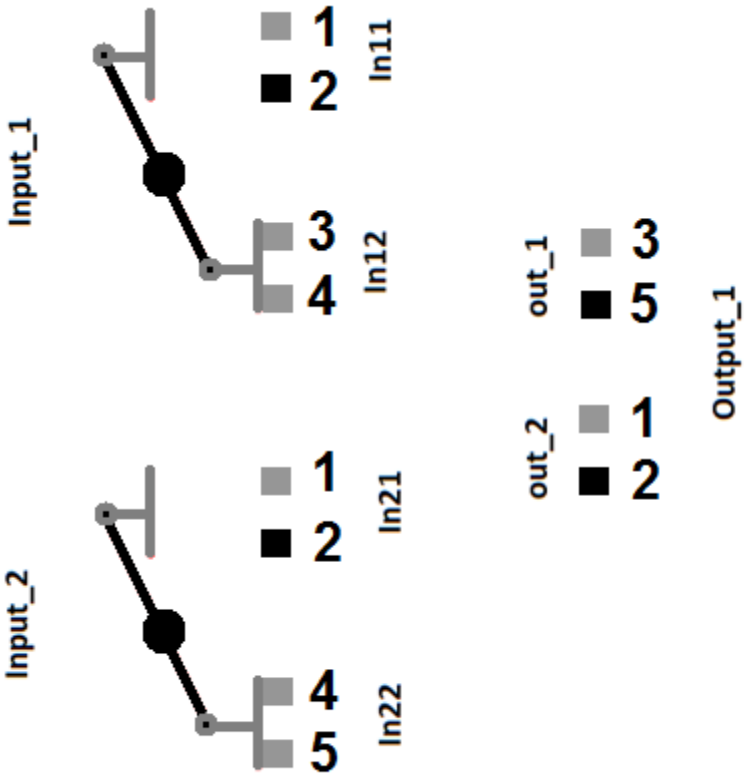

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.49

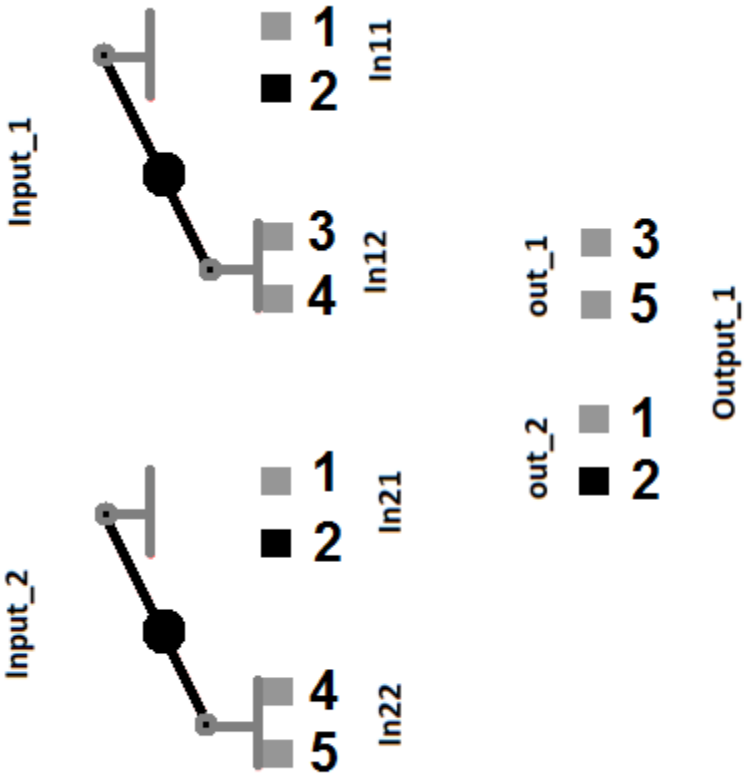

Input_1
1
2
In11
3
4
In12
Input_2
1
2
In21
4
5
In22
out_1
3
5
out_2
1
2
Output_1

Fig.50

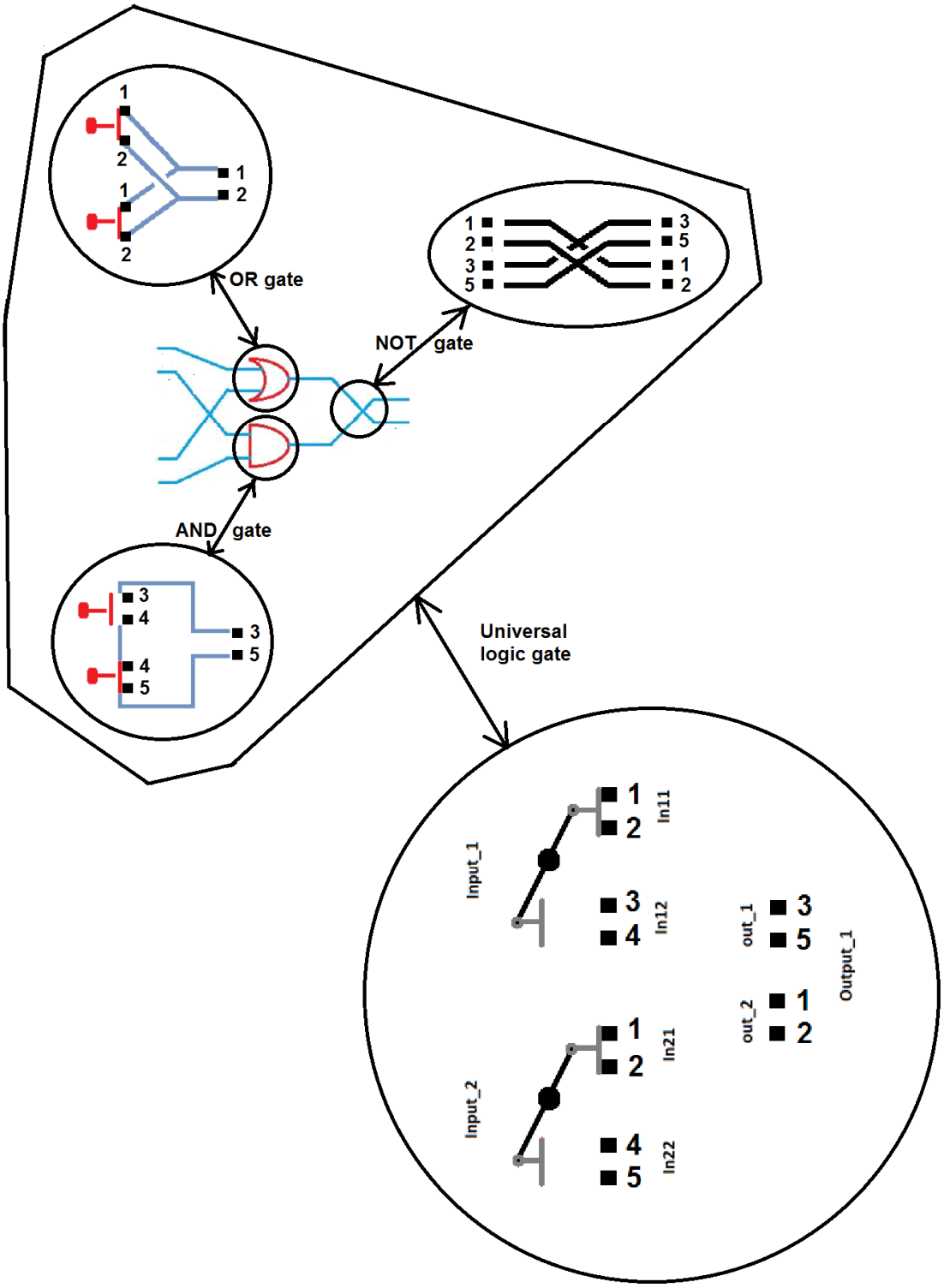

1
2
1
2
1
2
OR gate
1
2
3
5
3
5
1
2
NOT gate
AND gate
3
4
4
5
3
5
Universal
logic gate
Input_1
1
2
In11
3
4
In12
out_1
3
5
Output_1
out_2
1
2
Input_2
1
2
In21
4
5
In22

Fig.51

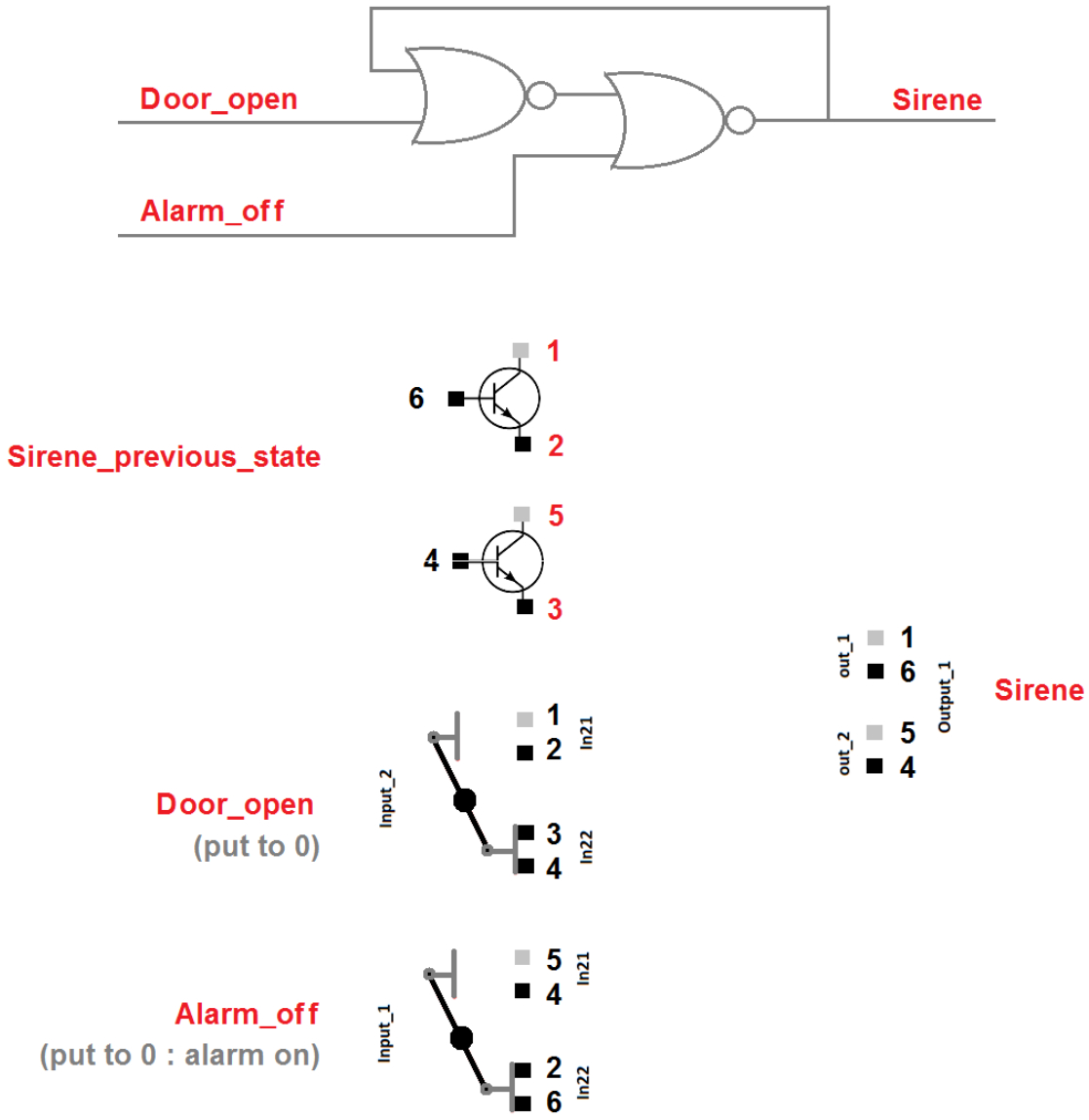

Door_open
Alarm_off
Sirene
Sirene_previous_state
Door_open
(put to 0)
Alarm_off
(put to 0 : alarm on)
Sirene
Input_2
Input_1
In21
In22
out_1
out_2
Output_1

Fig.52

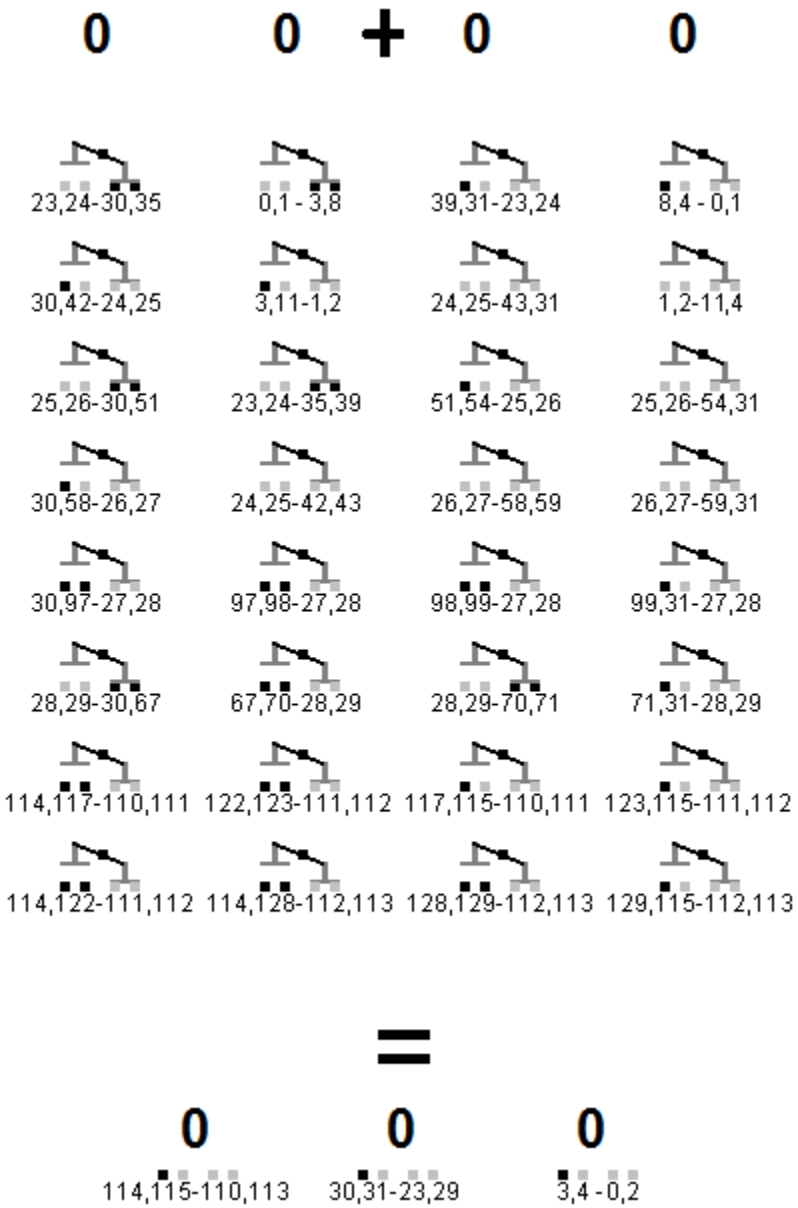

0
0
+
0
0
23,24-30,35
0,1 - 3,8
39,31-23,24
8,4 - 0,1
30,42-24,25
3,11-1,2
24,25-43,31
1,2-11,4
25,26-30,51
23,24-35,39
51,54-25,26
25,26-54,31
30,58-26,27
24,25-42,43
26,27-58,59
26,27-59,31
30,97-27,28
97,98-27,28
98,99-27,28
99,31-27,28
28,29-30,67
67,70-28,29
28,29-70,71
71,31-28,29
114,117-110,111
122,123-111,112
117,115-110,111
123,115-111,112
114,122-111,112
114,128-112,113
128,129-112,113
129,115-112,113
=
0
0
0
114,115-110,113
30,31-23,29
3,4 - 0,2

Fig.53

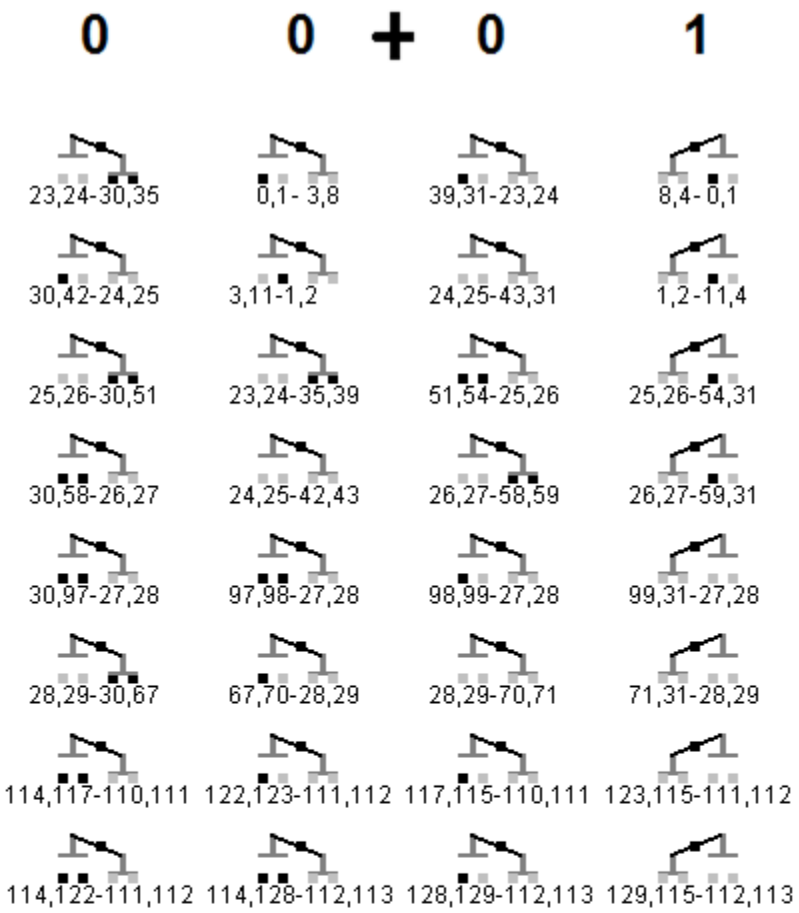

0
0
+
0
1
23,24-30,35
0,1- 3,8
39,31-23,24
8,4- 0,1
30,42-24,25
3,11-1,2
24,25-43,31
1,2-11,4
25,26-30,51
23,24-35,39
51,54-25,26
25,26-54,31
30,58-26,27
24,25-42,43
26,27-58,59
26,27-59,31
30,97-27,28
97,98-27,28
98,99-27,28
99,31-27,28
28,29-30,67
67,70-28,29
28,29-70,71
71,31-28,29
114,117-110,111
122,123-111,112
117,115-110,111
123,115-111,112
114,122-111,112
114,128-112,113
128,129-112,113
129,115-112,113
=
0
0
1
114,115-110,113
30,31-23,29
3,4- 0,2

Fig.54

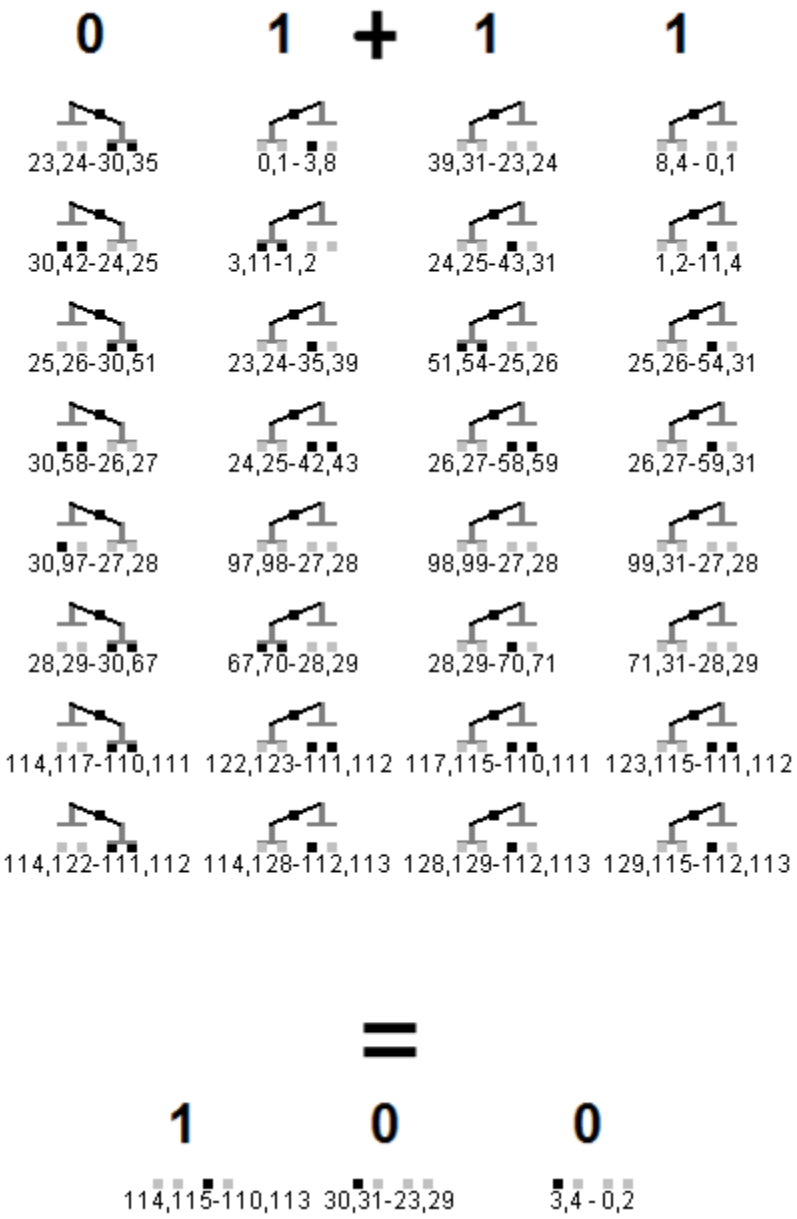

0
1
+
1
1
23,24-30,35
0,1-3,8
39,31-23,24
8,4-0,1
30,42-24,25
3,11-1,2
24,25-43,31
1,2-11,4
25,26-30,51
23,24-35,39
51,54-25,26
25,26-54,31
30,58-26,27
24,25-42,43
26,27-58,59
26,27-59,31
30,97-27,28
97,98-27,28
98,99-27,28
99,31-27,28
28,29-30,67
67,70-28,29
28,29-70,71
71,31-28,29
114,117-110,111
122,123-111,112
117,115-110,111
123,115-111,112
114,122-111,112
114,128-112,113
128,129-112,113
129,115-112,113
=
1
0
0
114,115-110,113
30,31-23,29
3,4-0,2

Fig.55

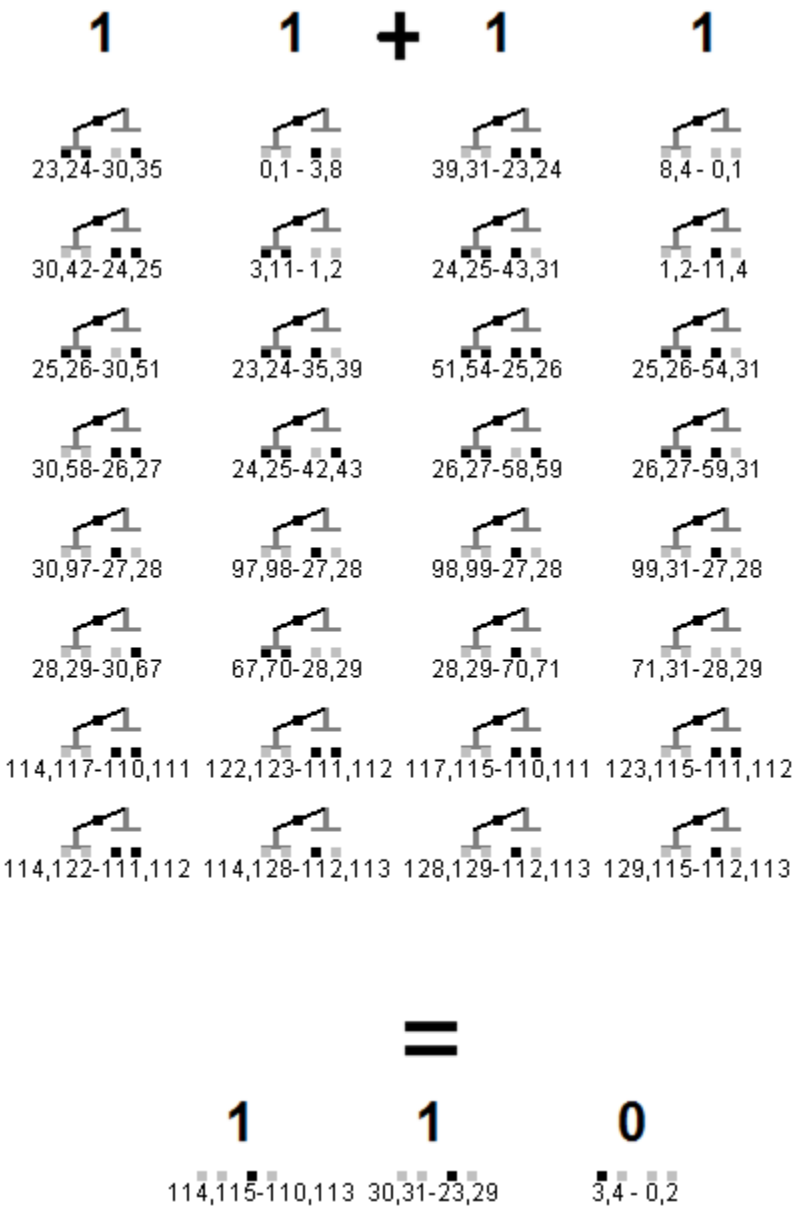

1
1
+
1
1
23,24-30,35
0,1 - 3,8
39,31-23,24
8,4 - 0,1
30,42-24,25
3,11- 1,2
24,25-43,31
1,2-11,4
25,26-30,51
23,24-35,39
51,54-25,26
25,26-54,31
30,58-26,27
24,25-42,43
26,27-58,59
26,27-59,31
30,97-27,28
97,98-27,28
98,99-27,28
99,31-27,28
28,29-30,67
67,70-28,29
28,29-70,71
71,31-28,29
114,117-110,111
122,123-111,112
117,115-110,111
123,115-111,112
114,122-111,112
114,128-112,113
128,129-112,113
129,115-112,113
=
1
1
0
114,115-110,113
30,31-23,29
3,4 - 0,2

Fig.56